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DIGITAL PHASE-LOCKED LOOP SPEED CONTROL FOR A BRUSHLESS  
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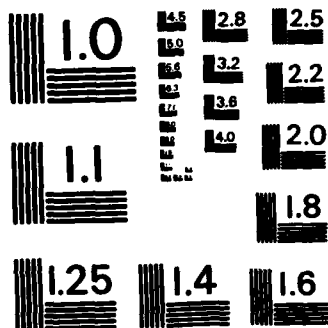
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## THESIS

DIGITAL PHASE-LOCKED LOOP SPEED CONTROL  
FOR A BRUSHLESS D.C. MOTOR

by

Michael Glynn Wise

June 1985

Thesis Advisor:

Alex Gerba, Jr.

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Digital Phase-locked Loop Speed Control  
for a Brushless D.C. Motor

by

Michael G. Wise  
Lieutenant, United States Navy  
B.E.T., Southern Technical Institute, 1978

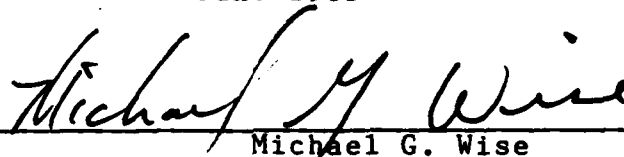
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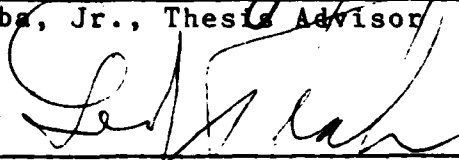
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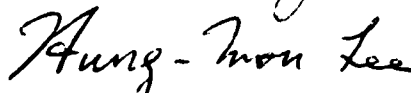
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## I. INTRODUCTION

Digital phase-locked loops (PLL) provide a means for very precise motor speed control. The speed accuracy is obtained by producing for each cycle of reference input one, and only one, cycle of output. Additionally, the digital components and shaft encoders used in PLL speed control are, to a large degree, insensitive to parameter variations due to component wear or environmental effects. Moore [Ref. 1] describes the design of a digital PLL speed control system, using the MC4044 phase frequency detector, to provide 0.002 percent speed regulation. The application of digital phase-locked loops to reference speeds is addressed by several authors [Refs. 2-5], in each case a constant reference is required to achieve accurate speed regulation. This thesis investigates the application of digital phase-locked loops to motor speed regulating and tracking of a variable and rapidly varying reference speed.

Digital phase-locked loop speed control of a brushless d.c. motor further enhances the advantage of electronic commutation. The elimination of mechanical commutation in the control system improves reliability and increases lifespan. Additionally, the excellent response time, small size and high efficiency of the brushless d.c. motor makes it a logical choice for a host of new applications. Of particular interest are flight control actuator systems of

Navy tactical missiles and space systems where reliability and long life are essential.

## II. PHASE-LOCKED LOOPS

Before describing the implementation of a digital phase-locked loop, using a synchronous up/down counter, a basic outline on phase-locked loop principles will be presented.

### A. PHASE-LOCKED LOOP PRINCIPLES

A basic phase-locked loop motor speed control system is shown in Figure 2.1.

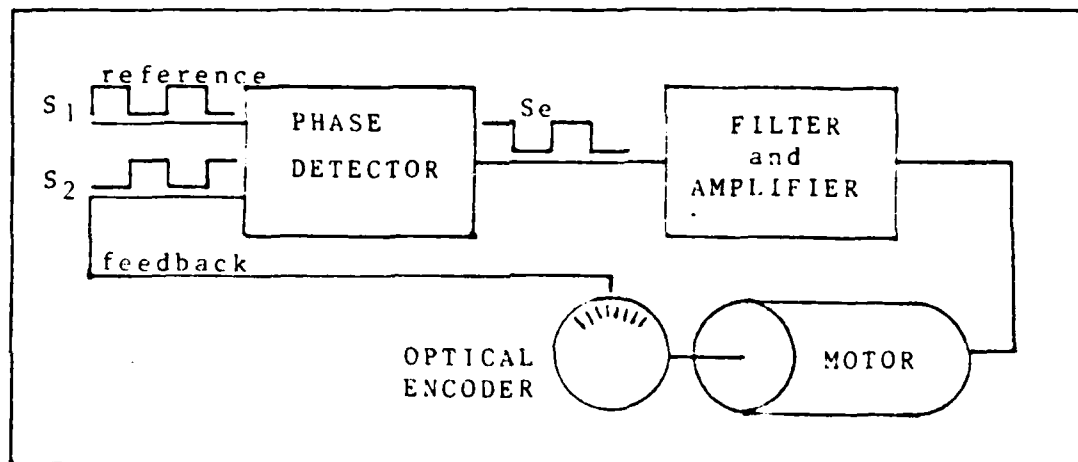


Fig. 2.1 Basic PLL Motor Speed Control System

The signals  $S_1$  and  $S_2$  are pulse trains generated by the reference frequency ( $f_1$ ) with phase ( $\theta_1$ ) and the motor feedback frequency (or speed) ( $f_2$ ) with phase ( $\theta_2$ ).  $S_2$  may be generated by an optical encoder mounted on the motor shaft or by Hall effect sensors mounted in the motor casing.

The phase error pulse train  $S_e$  is generated by the phase detector, it has a constant amplitude ( $\pm V_s$ ) and pulse width proportional to the phase difference:

$$\phi_e = \phi_1 - \phi_2 \quad (\text{eqn 2.1})$$

Under phase-locked conditions, that is  $f_1 = f_2$ , there is a synchronization, pulse for pulse, of  $S_1$  and  $S_2$ .  $S_e$  will then be a train of pulses of constant amplitude ( $V_s$ ) and pulse width ( $\phi_e/2\pi T$ ). Figure 2.2 illustrates the pulse trains for a phase-locked system. Should a disturbance cause an

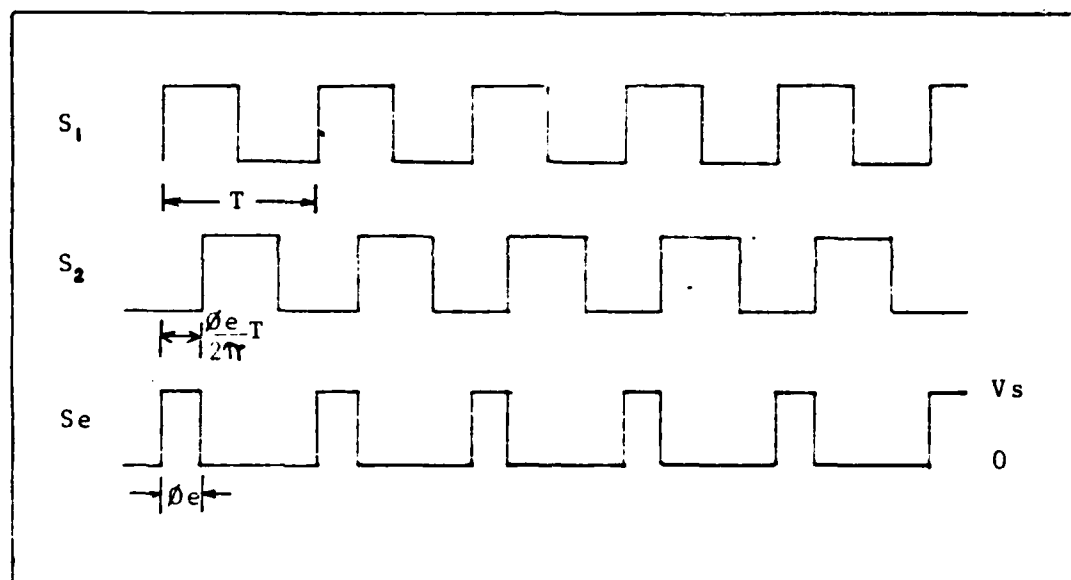


Fig. 2.2 Phase Detector Output,  $f_1 = f_2$   
with  $\phi_1$  Leading  $\phi_2$

increase or decrease in  $f_2$ , the pulse width and subsequently the average value of  $S_e$  will adjust accordingly.

The pulse train  $S_e$  can then be smoothed by a lowpass filter. The filtered signal is then the average or d.c. component of  $S_e$ .

Now consider the case when the system is not in phase-lock. For example,  $f_1 > f_2$ , the pulse trains for  $S_1$ ,  $S_2$  and  $S_e$  are shown in Figure 2.3. From Figure 2.3, it can be seen

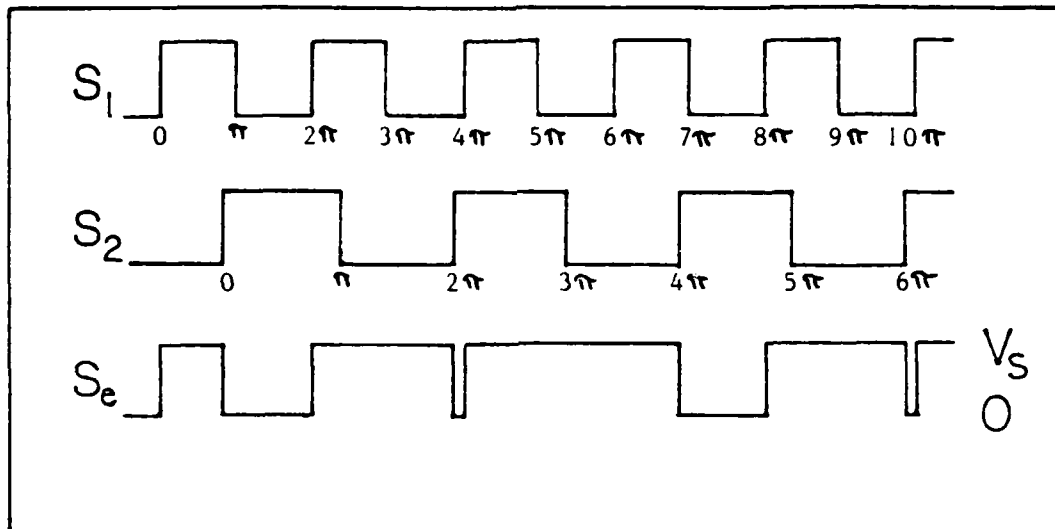


Fig. 2.3 System Not in Phase-lock,

that with each successive cycle of input the pulse width of  $S_e$  increases unless  $f_2$  increases. In order for the phase-locked loop to acquire "lock", three conditions must be met [Ref. 6]:

1. The system must be stable.
2. The frequency of the effective error signal should be within the bandwidth of the system.
3. The average value of the phase detector's output, plus any amplification and bias applied, must be sufficiently large to drive the motor at the reference frequency.

The average value of the phase detector output, when phase-locked, is shown in Figure 2.4 as a function of phase

error. Figure 2.4 illustrates the linear relationship between the phase error and the output of the phase detector within the region  $-2\pi$  to  $2\pi$ .  $V_S$  represents the maximum output voltage of the phase detector. This model was originally suggested by Moore [Ref. 1] and can be used to determine the range of frequencies over which the phase detector can achieve lock.

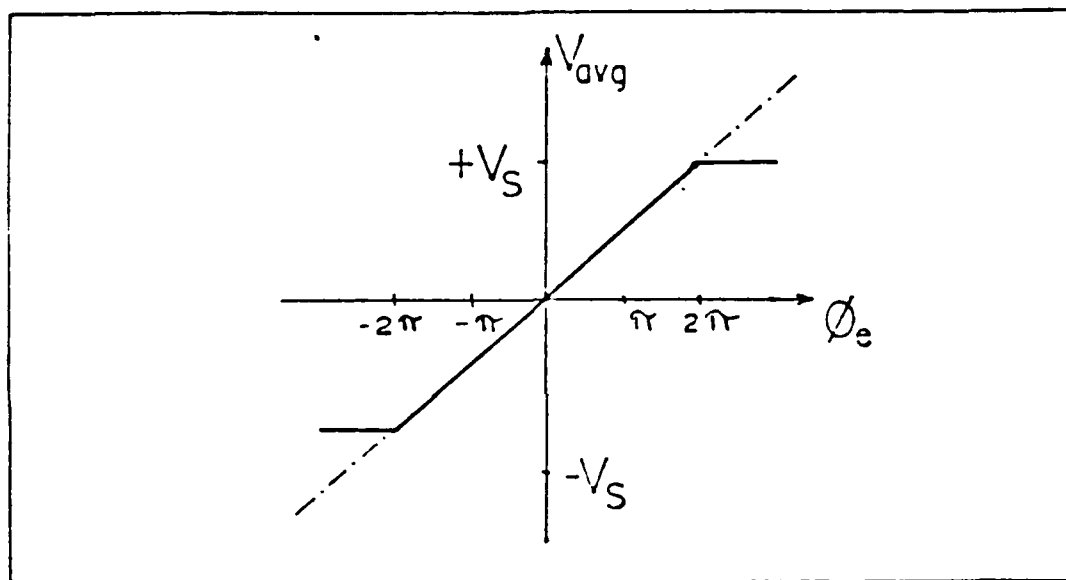


Fig. 2.4 Phase Detector's Output as a Function of Phase Error

In order to evaluate the frequency range over which the phase detector can operate, a constant,  $K$ , is defined to be the gain of the motor loop in (rad/sec)/volt. The frequency of  $S_2$  will be

$$f_2 = f_0 + K V_{avg}/2\pi \quad (\text{eqn 2.2})$$

where  $f_0$  is a center frequency due to a bias voltage. The

maximum of  $V_{avg}$  occurs when  $\phi_e = 2\pi$ , then  $V_{avg} = +V_s$ . Similarly for  $\phi_e = -2\pi$ , then  $V_{avg} = -V_s$ . The lock range is then

$$f_0 - K V_s / 2\pi \leq f_2 \text{ (lock)} \leq f_0 + K V_s / 2\pi \quad (\text{eqn 2.3})$$

which is defined to be the range of frequencies that the system can operate over while maintaining phase lock [Ref. 3].

## B. DIGITAL PHASE DETECTOR

In a digital phase detector, the phase difference is measured by the time difference between the rising (or trailing) edges of  $S_1$  and  $S_2$ . A state diagram of a digital circuit which senses the leading edges of the input signals and changes states accordingly, as suggested by Tal [Ref. 2], is shown in Figure 2.5. A rising edge on  $S_1$  ( $S_1 \uparrow$ ) shifts the state to the right, a rising edge on  $S_2$  ( $S_2 \uparrow$ ) shifts the state to the left. If the phase detector is in the  $\pm V_s$  state

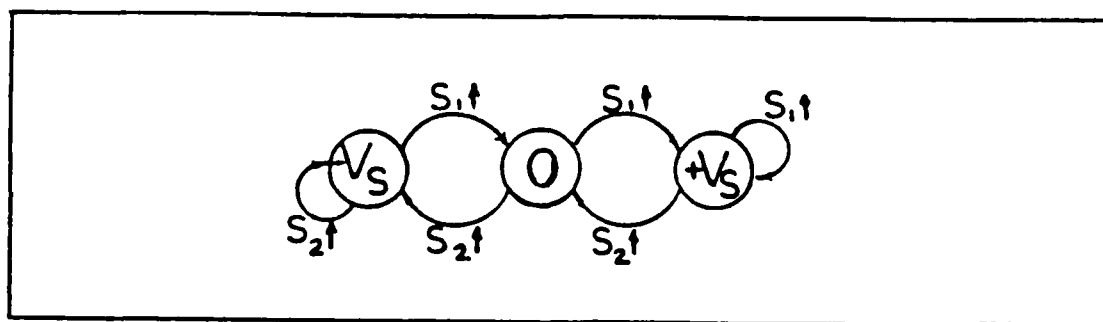


Fig. 2.5 Three-state Diagram of Digital Phase Detector

and a rising edge on  $S_1$  or  $S_2$  occurs prior to a shift to the "0" state, the state remains the same. For the three-state

phase detector, five conditions can exist:

1.  $f_1 = f_2$ ,  $S_1$  leads  $S_2$  the output switches between 0 and  $+V_S$ .
2.  $f_1 = f_2$ ,  $S_2$  leads  $S_1$ , the output switches between  $-V_S$  and 0.
3.  $f_1 = f_2$ ,  $S_1$  is in phase with  $S_2$  and the output is zero.
4.  $f_1 > f_2$ , the output switches between zero and  $+V_S$  with more time spent in the  $+V_S$  state.
5.  $f_2 > f_1$ , the output switches between  $-V_S$  and zero with more time spent in the  $-V_S$  state.

The three-state phase detector is subject to a false lock hazard because it cannot encode phase errors greater than  $2\pi$ . A false lock condition is illustrated in Figure 2.6. Note the region labeled false lock in Figure 2.6.  $S_1$  has a

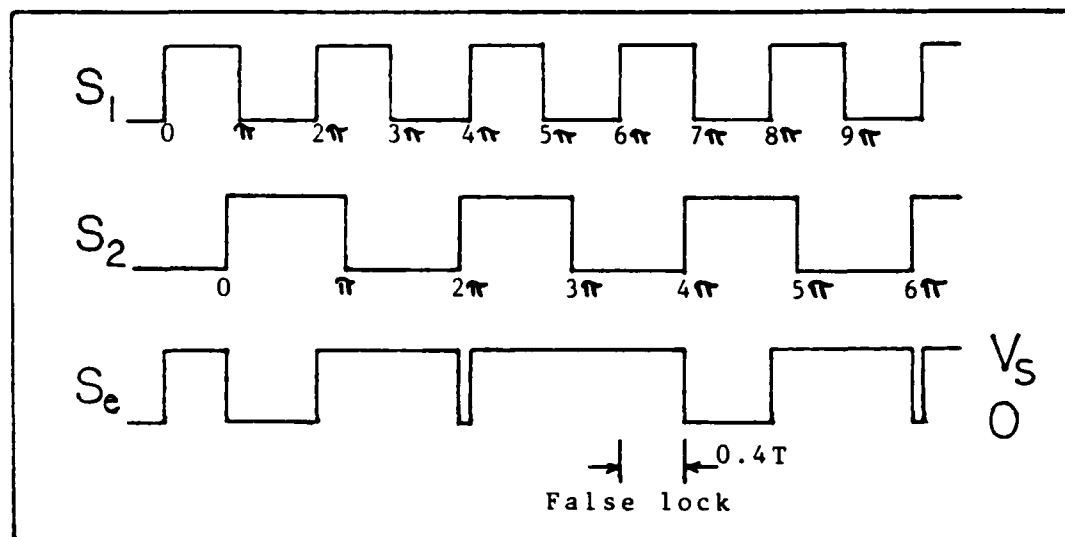


Fig. 2.6 False Lock Hazard

leading edge which rises when its phase is  $6\pi$ , at that time the phase of  $S_2$  is  $3.6\pi$ . The phase error, from equation 2.1 is



$$\phi_e = 6\pi - 3.6\pi = 2.4\pi \quad (\text{eqn 2.4})$$

The pulse width of the phase detector, in terms of the reference T, should be

$$\text{Pulse width} = \phi_e / 2\pi T = 1.2T \quad (\text{eqn 2.5})$$

This, however, is not in agreement with the mechanics of a three-state phase detector. Because the phase detector is in the  $+V_S$  state when  $S_1$  rises at  $6\pi$ , it simply remains in the  $+V_S$  state. When  $S_2$  rises at  $4\pi$ , the phase detector transitions to the "0" state. The phase detector has a pulse width, from Figure 2.6, of  $0.4T$  in the region of false lock. The average value of the phase detector over the fourth time period, where the false lock occurs, is

$$V_{\text{avg}} = \frac{1}{2\pi} \int S_e d\phi = \frac{1}{2\pi} \int_{6\pi}^{6.4\pi} V_S d\phi + \frac{1}{2\pi} \int_{6.4\pi}^{8\pi} 0 d\phi = 0.2V_S \quad (\text{eqn 2.6})$$

From equation 2.4 the phase error in the false lock region is greater than  $2\pi$ . According to Figure 2.4, the average output of the phase detector for phase error greater than  $2\pi$  should be  $+V_S$ , however from equation 2.6  $V_{\text{avg}}$  is only  $0.2V_S$ . Therefore, a false lock condition can exist.

### C. n-STATE PHASE FREQUENCY DETECTOR

A method for eliminating the false lock hazard is suggested by Whitaker and Tal [Ref. 3]. The approach is to increase the number of states available to the phase

detector. A state diagram for a  $n$ -state phase detector is shown in Figure 2.7. The  $n$ -state phase detector provides a

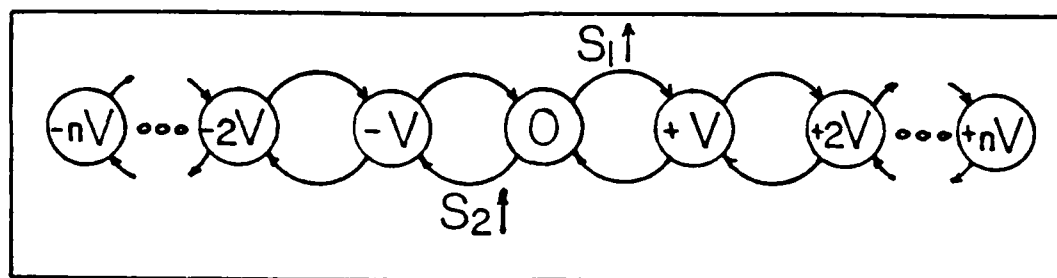


Fig. 2.7 State Diagram for  $n$ -State Phase Detector

mechanism to encode phase differences greater than  $2\pi$ . As with the three-state phase detector, the time duration between rising edges of  $S_1$  and  $S_2$  is a measure of phase difference (when less than  $2\pi$ ). With the  $n$ -state phase detector, however, a phase difference greater than  $2\pi$  is encoded by a transition to a higher state. Each transition to a higher state is equivalent to an integer multiple of  $2\pi$ .

To illustrate how the  $n$ -state phase detector avoids the false lock hazard of the three-state phase detector, observe Figure 2.8. The pulse trains in Figure 2.6 are shown again in Figure 2.8, this time with a  $n$ -state phase detector. Note that when  $S_1$  leads  $S_2$  by more than  $2\pi$ , it is encoded by an increase in amplitude in the phase detector's output. Comparing the output of the  $n$ -state phase detector, Figure 2.8, to the three-state phase detector, Figure 2.6, reveals

the advantages of an increase in available states. For the n-state phase detector, in the time period of interest, the

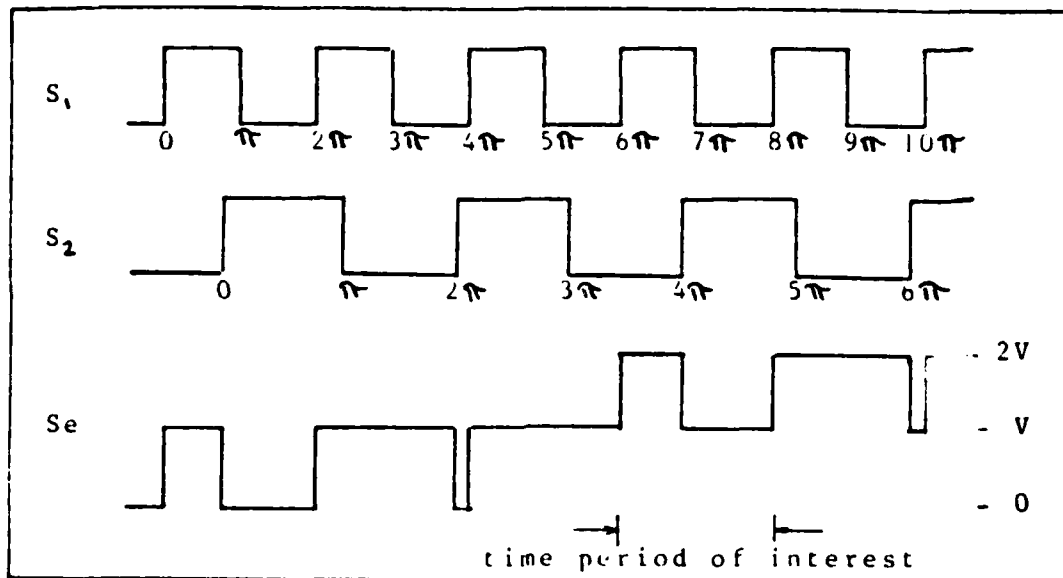


Fig. 2.8 Output of n-State Phase Detector

pulse duration between rising edges of  $S_1$  and  $S_2$  has not changed, however it has increased in amplitude. Therefore, the average value during the period will be

$$V_{avg} = \frac{1}{2\pi} \int_{6\pi}^{8\pi} S_e d\phi = \frac{2V_s}{2\pi} \int_{6\pi}^{6.4\pi} d\phi + \frac{V_s}{2\pi} \int_{6.4\pi}^{8\pi} d\phi = 1.2V_s \quad (\text{eqn 2.7})$$

Examination of Figure 2.4 indicates this would be the desired average value for a phase error of  $2.4\pi$ , if the phase detector was not limited to  $\pm V_s$ .

### III. SYNCHRONOUS UP/DOWN COUNTER IN PHASE-LOCKED LOOPS

Implementation of the  $n$ -state phase frequency detector, as suggested in Chapter 2, is quite straightforward. With an up/down counter and D/A converter (DAC), the state diagram in Figure 2.7 can be easily realized. In operation, the leading edge of a reference signal pulse ( $S_1$ ) causing a count up (state transition) and a leading edge of the feedback signal ( $S_2$ ) causing a count down. The action of such a device is described by Geiger [Ref. 4] to be a frequency error integrator.

The action of the up/down counter is a stepwise increase or decrease in voltage with each leading edge of the input signals. Clearly, if a difference exists between the frequencies of  $S_1$  and  $S_2$ , the output of the up/down counter will adjust according to the more frequently occurring pulse train. If the output voltage of the up/down counter is applied to a d.c. motor, with the motor's speed as the feedback signal ( $S_2$ ), then the motor's speed will adjust with the increase (decrease) of voltage until the frequency error is zero. In this sense the up/down counter can be considered a frequency detector.

Once the two input frequencies are nearly equal, the up/down counter will alternate between two values, changing with each input signal leading edge. The output would be a pulse train of constant frequency and pulse width, with an

average value sufficient to drive the motor at the reference frequency. Should a frequency difference occur, the pulse width would adjust accordingly as in a phase detector, or if the frequency error continued, the counter would eventually change count.

#### A. UP/DOWN COUNTER AS A FREQUENCY ERROR INTEGRATOR

The input pulse trains  $S_1$  and  $S_2$  and the output of an up/down counter-DAC are shown in Figure 3.1. The example in Figure 3.1 assumes the feedback signal  $S_2$  comes from a motor initially at rest which accelerates to a locked condition.

As can be seen in Figure 3.1, with an initial large difference between  $f_1$  and  $f_2$ , the counter counts up rapidly. As the frequency difference becomes small, the rate at which the counter increases decreases. The effect is similar to a frequency error integrator.

The output of the up/down counter-DAC can be expressed as

$$\Delta V_0 = K_c (\Delta \text{count}) \quad (\text{eqn 3.1})$$

where  $\Delta \text{count}$  = change in counter

$K_c$  = incremental voltage of each count

$\Delta V_0$  = change in output voltage of DAC

also

$$K_c = V_{\max} / \text{Count}_{\max} \quad (\text{eqn 3.2})$$

where  $V_{\max}$  = maximum DAC voltage

$\text{Count}_{\max}$  = maximum count available to the  
the counter (8 bit counter = 255)

# UP/DOWN COUNTER INTEGRATOR VOLTS VS TIME

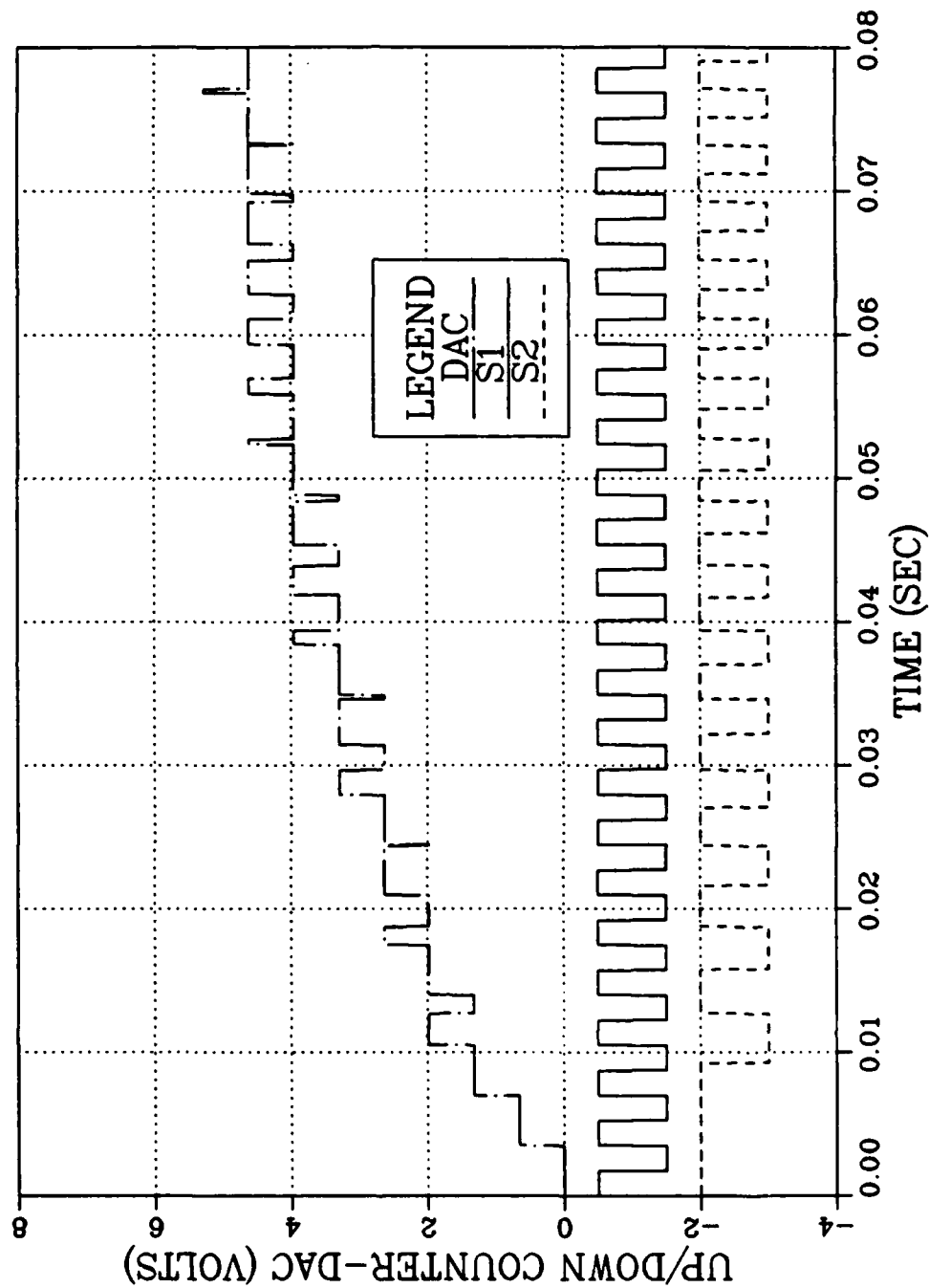


Fig. 3.1 Up/Down Counter as a Frequency Error Integrator

The change in count in a time period is the number of cycles of  $S_1$  less the number of cycles of  $S_2$ .

$$\Delta \text{Count} = (f_1 - f_2) \Delta t \quad (\text{eqn 3.3})$$

Substituting equation 3.3 into 3.1 yields

$$\Delta V_0 = K_c (f_1 - f_2) \Delta t \quad (\text{eqn 3.4a})$$

or

$$\Delta V_0 / \Delta t = K_c (f_1 - f_2) \quad (\text{eqn 3.4b})$$

taking the limit as  $t \rightarrow 0$

$$\lim_{t \rightarrow 0} \Delta V_0 / \Delta t = dV_0 / dt = K_c (f_1 - f_2) \quad (\text{eqn 3.5})$$

and integrating both sides with respect to time

$$V_0 = K_c \int (f_1 - f_2) dt + C \quad (\text{eqn 3.6})$$

From equation 3.6 the up/down counter is a true frequency error integrator, with resolution subject to the step size  $K_c$ .

## B. THE UP/DOWN COUNTER AS A PHASE FREQUENCY DETECTOR

When the reference and feedback frequencies are very nearly equal, the counter will hold its count with a duty cycle in its least significant bit (LSB). The duty cycle is a result of the counter transitioning on alternating leading edges of  $S_1$  and  $S_2$ . The count stored by the up/down counter is sufficient, within the counter resolution  $K_c$ , to drive the motor at the reference frequency.

With the frequency difference resolved by the up/down counter, the phase error is measured by the time duration of

the LSB in its high state. The output of the up/down counter under "frequency locked" conditions is shown in Figure 3.2.

The average voltage output of the up/down counter-DAC will be

$$V_{avg} = V_n + T_d/T \cdot (V_{n+1} - V_n) \quad (\text{eqn 3.7})$$

where  $T_d$  is the time duration of the LSB in  $V_{n+1}$  and  $T$  is the period of the reference frequency.

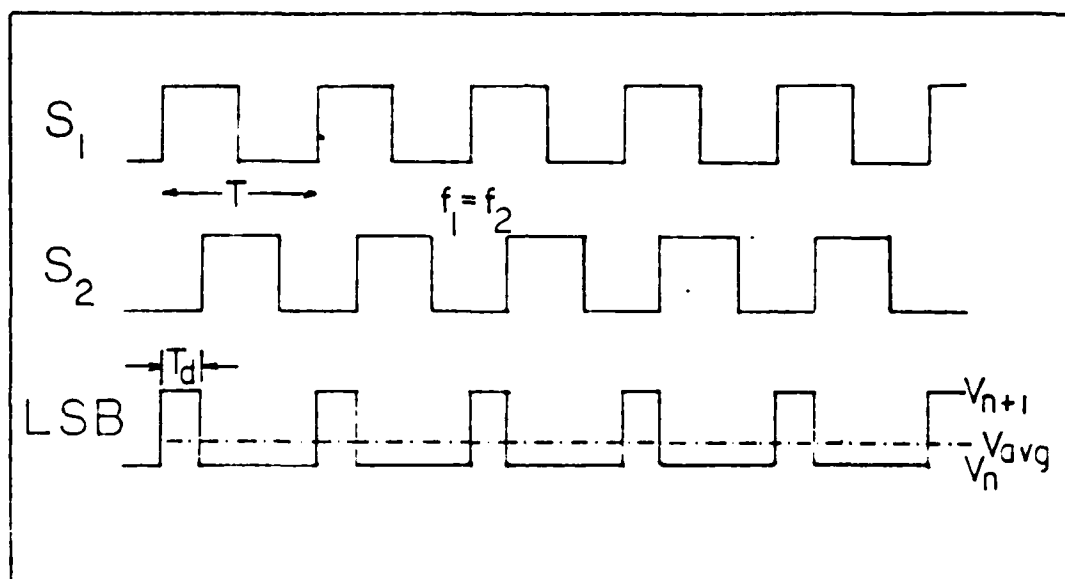


Fig. 3.2 Up/down Counter-DAC Output

Figure 3.2 and equation 3.7 illustrate the phase lock characteristics of the up/down counter. The discrete voltages  $V_n$  and  $V_{n+1}$  do not provide the exact voltage necessary to drive the motor at the reference frequency. The duty cycle of the LSB provides the incremental adjustment



between  $V_n$  and  $V_{n+1}$  to satisfy the average voltage requirements for a given motor speed and torque.

#### C. IMPROVED TIME RESPONSE OF THE UP/DOWN COUNTER PFD

In choosing the up/down counter step size,  $K_c$  (volts/count), consideration must be given to the trade off between:

1. Integration and frequency lock resolution.
2. Rate at which counter can change voltage levels.

Clearly, if  $K_c$  is very small, the up/down counter could resolve the discrete voltage levels  $V_n$  and  $V_{n+1}$  in Figure 3.2 to an almost insignificant difference. However, for a change in reference frequency or a torque load induced frequency error, the counter must count up (or down) to a new operating value. In this case a large value of  $K_c$  is desired. With a large  $K_c$  the counter could change to the new operating value in only a few cycles, then rely on the duty cycle of the LSB to compensate for the loss in resolution.

The primary purpose of the up/down counter-DAC is to provide the d.c. voltage required to drive the motor at the reference speed. With this in mind, an alternative approach to improving the time response of the up/down counter exists. From Figure 3.1 any down count when  $f_2 < f_1$  only slows the counter from reaching the required count value. Likewise, for  $f_2 > f_1$ , a count up is undesirable. At the expense of additional hardware to sense the over/under frequency condition and logic circuits to enable and disable the

counter accordingly, the counter's time response can be significantly improved.

In order to provide the necessary logic signal to enable/disable the counter's up/down inputs, digital frequency to voltage converters (F/V) must be added to the system. Referring to Figure 3.3, National Semiconductor AN-210 frequency-to-voltage converters, which employ phase-locked loop techniques, may be used to provide precise frequency-to-voltage conversion. The voltage output of the F/V converters, through a differential amplifier with gain  $K_p$ , provides a signal which is positive if  $f_1 > f_2$  and negative if  $f_2 > f_1$ . This signal, through logic gates, inhibits the appropriate counter input. The inhibit is accomplished by combining through OR gates a steady high logic level with the input pulse train to be disabled. Figure 3.3 illustrates the basic implementation of the circuit.

The addition of the F/V converters and differential amplifier provides an additional advantage. They can be used to provide a proportional gain path. The addition of a proportional gain path enhances the overall stability of the system and provides a source of drive when a large frequency error exists. This is an important factor since the up/down counter no longer acts as a frequency error integrator until the error is very small. The action of an up/down counter with logic controlled count enable/disable cutouts is shown in Figure 3.4. As in Figure 3.1, the example assumes the

signal  $S_2$  comes from a motor initially at rest which accelerates to a locked condition.

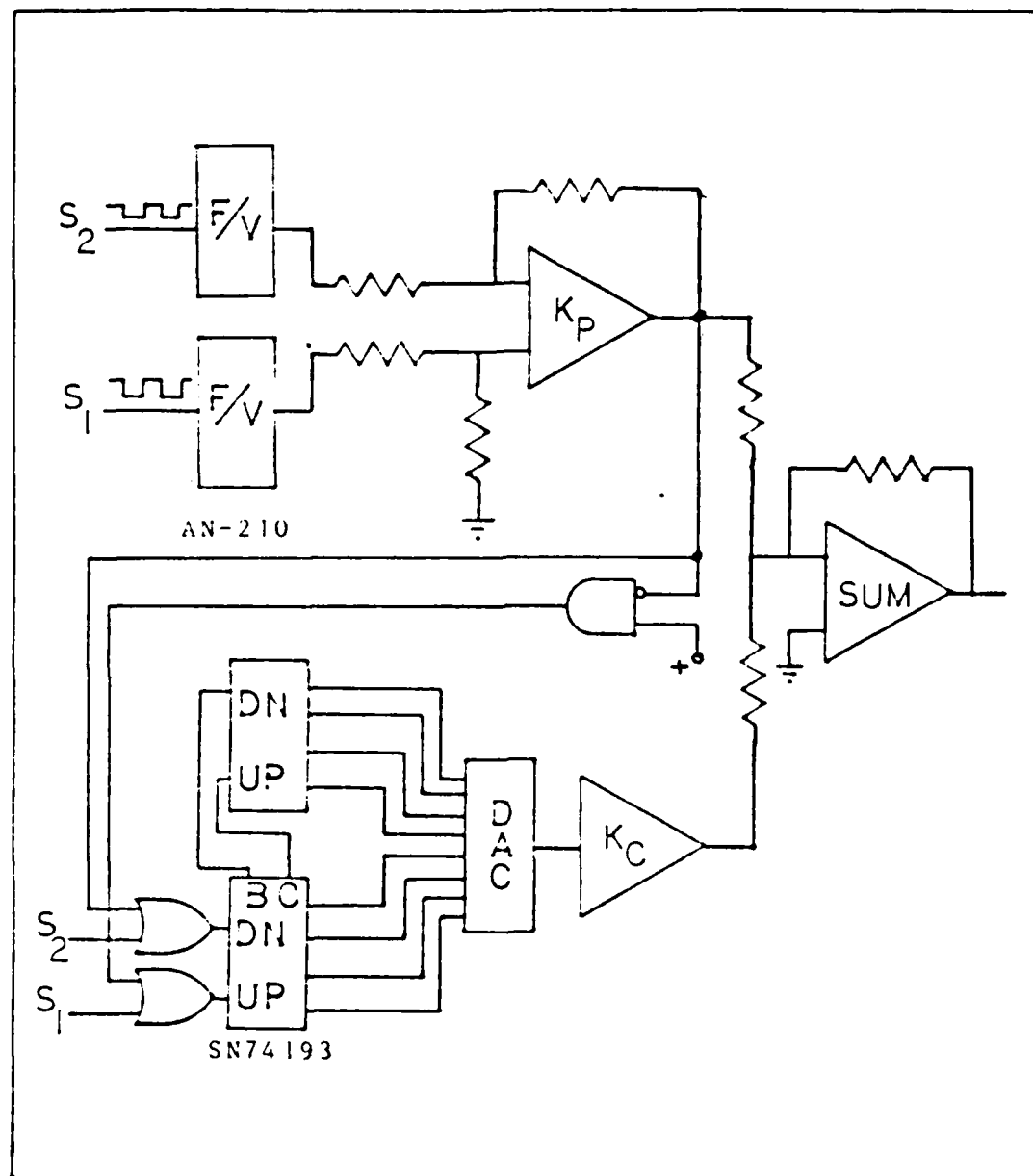


Fig. 3.3 Up/down Counter with Logic Controlled Count Enable/Disable

The initial idea to include the logic controlled count enable/disable in the up/down counter must be categorized as

an intuitive approach. The idea occurred while observing the behavior of the up/down counter in a computer simulated PLL scheme with a ramped reference frequency. The response of the up/down counter-DAC to a ramped reference frequency and subsequent motor speed response are shown in Figure 3.5.

As can be seen in Figure 3.5 as the reference frequency begins to ramp up, the counter begins to increase at an exponential rate. The motor speed follows the exponential rise of the counter and speed tracking is lost until the reference frequency becomes constant again.

Various filters were initially tried in an attempt to inhibit the up/down counter's exponential rise, these proved to be unsuccessful. Finally in a "brute force" attempt, logic cutouts were included in the simulation model. The effect was immediately noticeable, the system began to track variable reference frequencies with negligible error. Additionally, its response to torque disturbances was significantly faster. An example of the PLL system response with the logic cutouts is shown in Figure 3.6.

The addition of logic controlled, up/down count, enable/disable introduces yet another nonlinear element to the discrete nature of the digital PLL. And indeed makes an analytical solution to the behavior of the control system very difficult. A design procedure based on a linearized model and computer simulation is presented in Chapter 5.

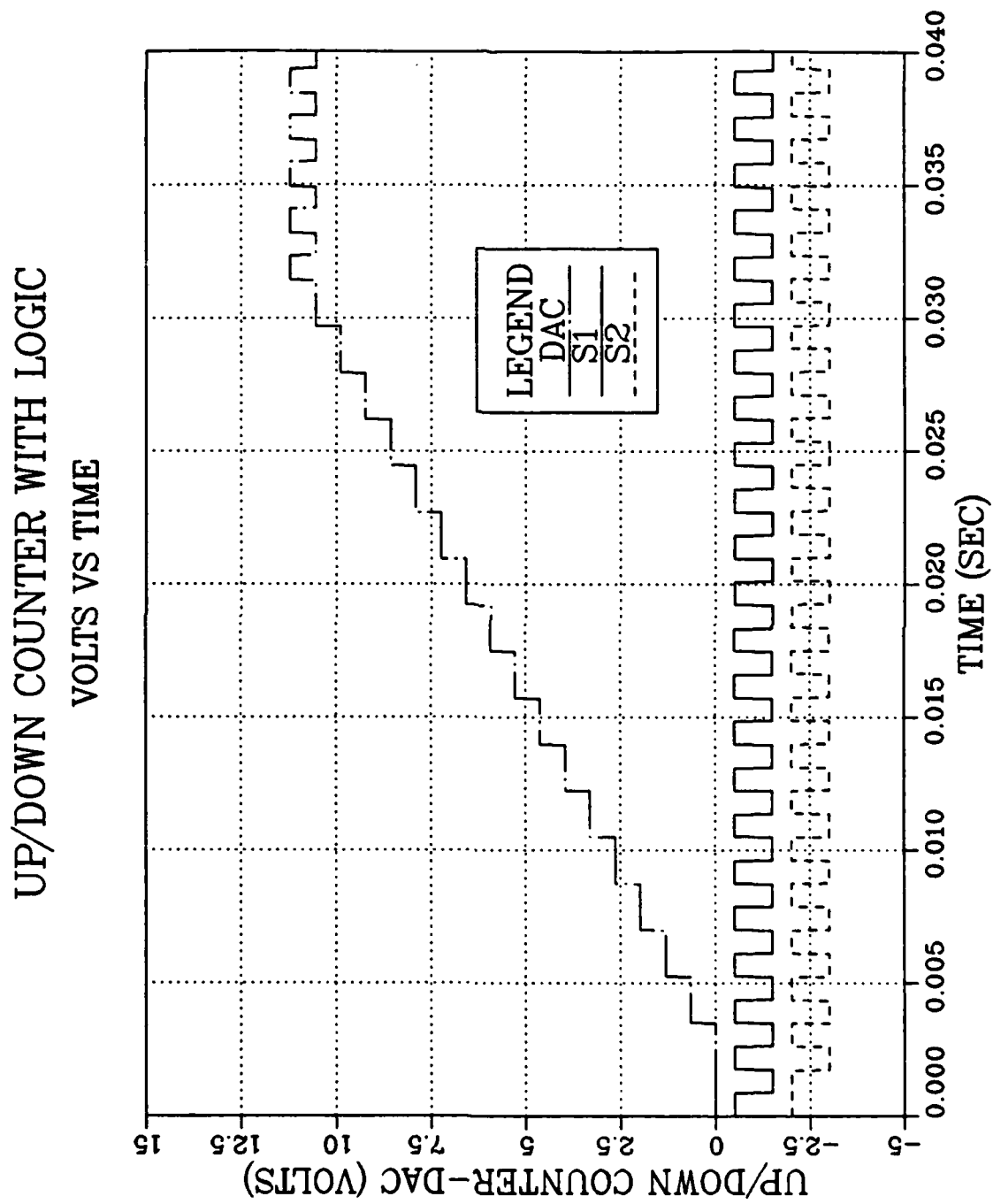


Fig. 3.4 Up/Down Counter with Logic Controlled Count Enable/Disable

# PLL MOTOR SPEED CONTROL SPEED AND DAC VOLTS

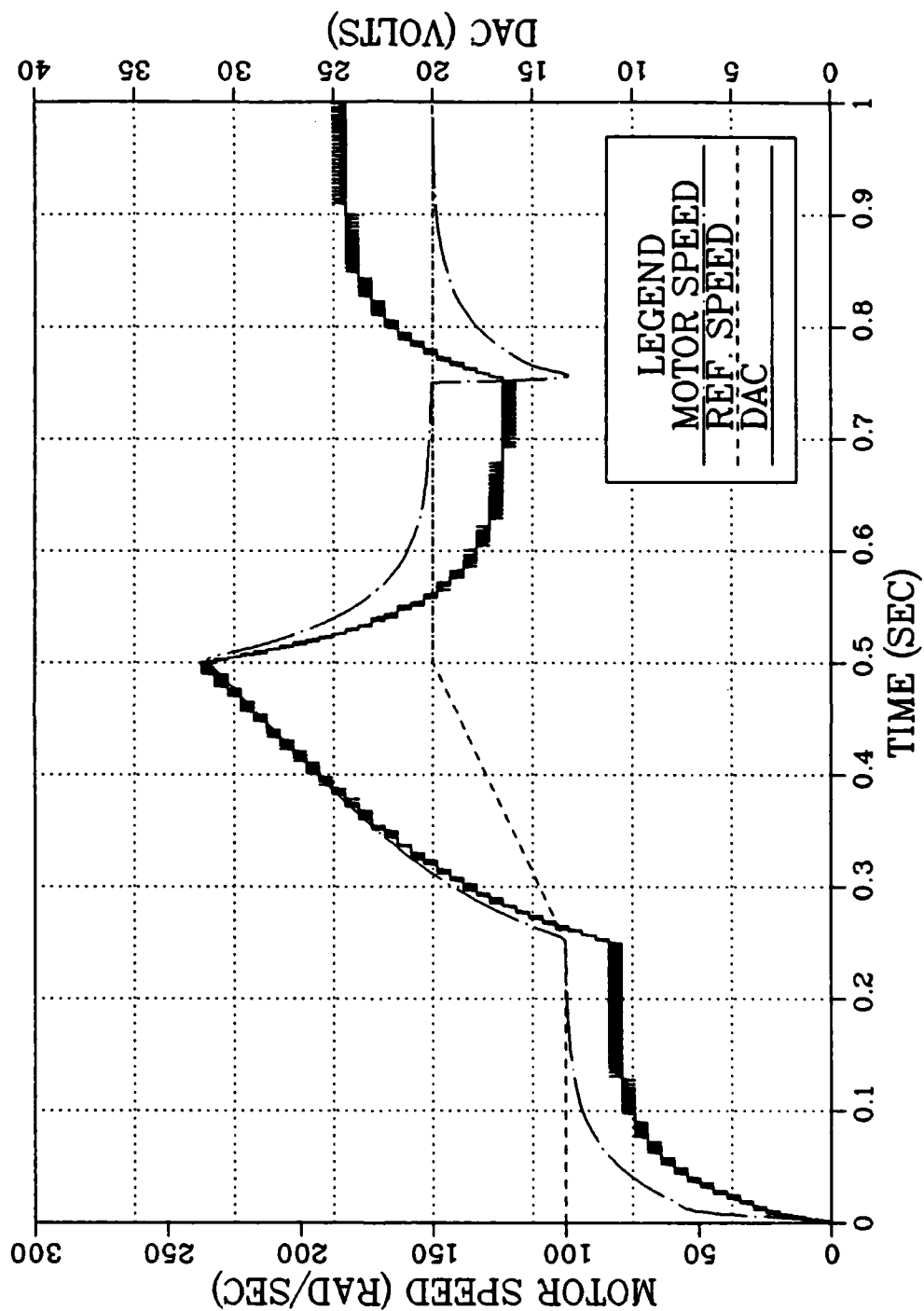


Fig. 3.5 PLL Control Response to Ramp Input and Torque Load (at  $t = 0.75$  sec)

# PLL MOTOR SPEED CONTROL SPEED AND DAC VOLTS

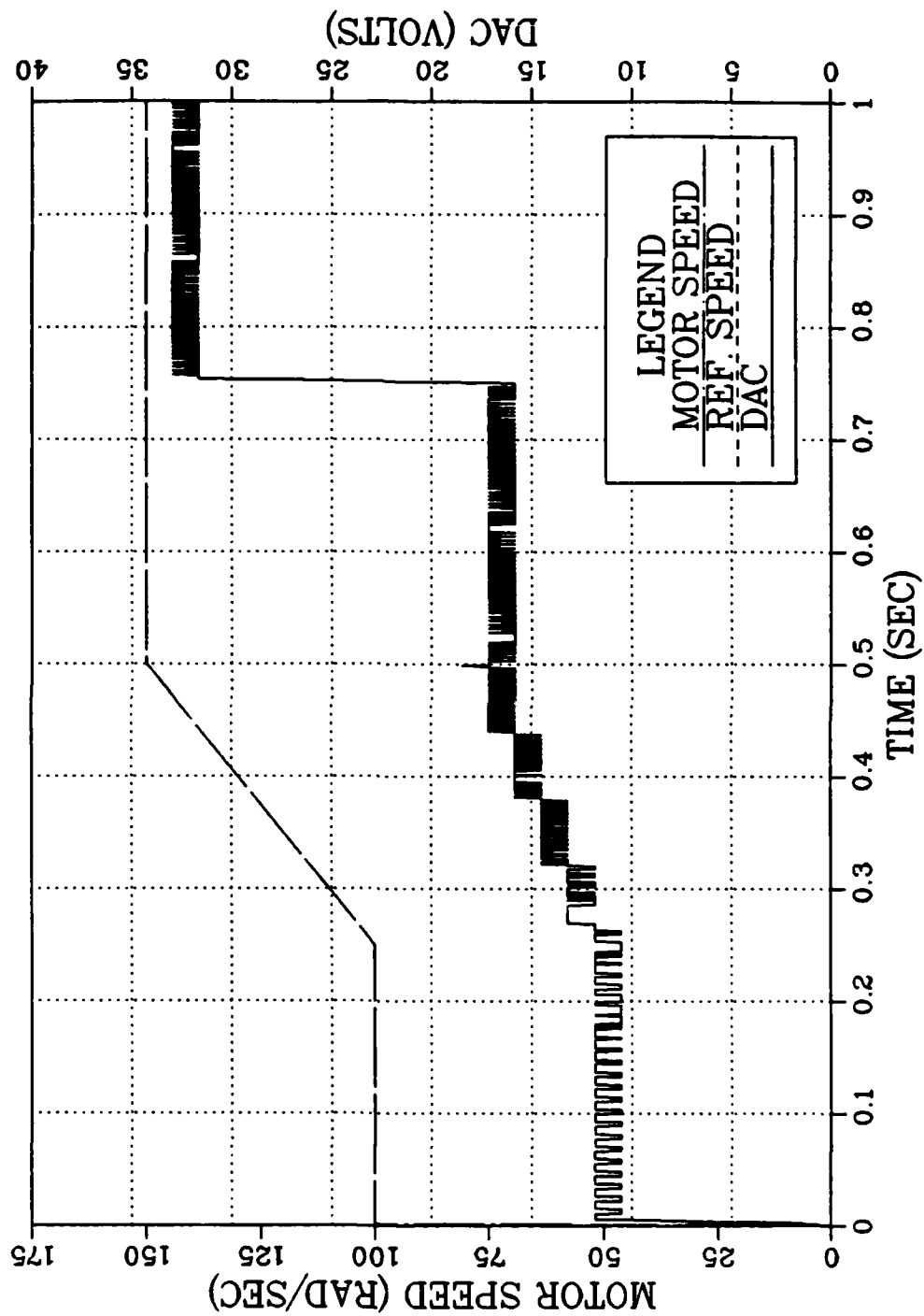


Fig. 3.6 PLL System Response with Logic Controlled Count Enable/Disable (90 oz-in torque at  $t = 0.75$ )

#### IV. BRUSHLESS D.C. MOTOR AND OPTICAL ENCODER

The brushless d.c. motor has the same torque-speed characteristics as the conventional d.c. permanent magnet motor; what sets it apart is its lack of mechanical commutation components. It also has the advantages of [Ref. 7]:

1. Increased mechanical power with decreased size.
2. Better heat dissipation capability.

##### A. BRUSHLESS D.C. MOTOR PRINCIPLES

The elimination of mechanical commutation components by means of electronic switching means improved reliability and longer life. Additionally, elimination of brushes allows the motor to be used in explosive environments or where carbon dust could be detrimental to adjacent components.

In a brushless d.c. motor, permanent magnets are typically mounted on the rotor shaft and windings are placed in an external, slotted stator. This configuration allows for a low rotor moment of inertia and a more direct path for heat dissipation to the environment. It also means a more complex electronics package is required to provide current switching in the motor's windings.

The basic principle of brushless commutation is to electronically switch current to the appropriate stator winding. The logic signals for switching to the appropriate



winding are provided by shaft positions sensors, which can be Hall effect sensors or optical encoders for example. A more detailed analysis of brushless commutation was reported by MacMillan [Ref. 8].

## B. OPTICAL ENCODER

The basic optical encoder is shown in Figure 4.1. The disk is a flat plate fixed to the motor shaft with  $N$  slots. The number of slots,  $N$ , can be as few as desired, however,

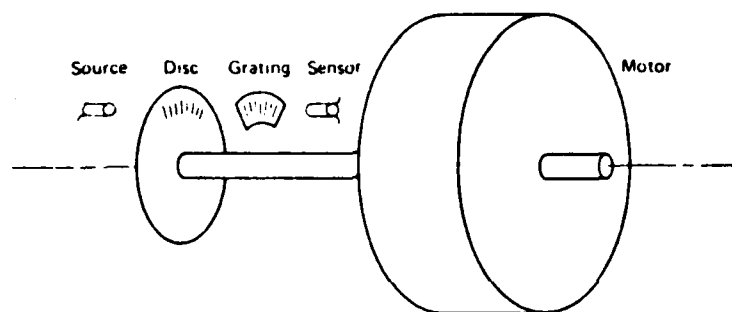


Fig. 4.1 Exploded View of An Optical Tachometer

there is a practical upper limit on  $N$  for a given disk diameter. There is also an ultimate limit on  $N$  due to the wavelength of light. Typically for a 2.5 inch diameter disk the maximum line density is 5000.

The grating shown in Figure 4.1 is necessary when the sensor size is large in comparison to the slot spacing. An example of the need for grating is illustrated in Figure 4.2(a). In this example the sensor cannot distinguish when a slot passes between the light source and the sensor. With a

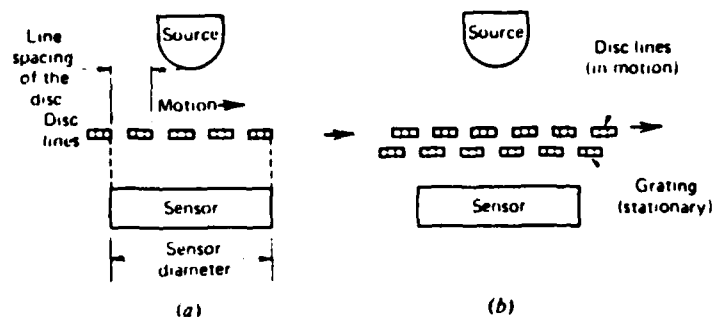


Fig. 4-2 (a) Sensor cannot distinguish change in light intensity with each passing slot.  
 (b) Grating effectively blanks light with each passing slot.

grating, which has the same line spacing as the disk, held stationary between the disk and the sensor, the light is completely blanked out with each passing slot as shown in Figure 4.2b.

The sensor transmits a pulse train with the frequency

$$f_{tach} = N f_{shaft} \quad (\text{eqn 4.1})$$

where  $f_{tach}$  = frequency of the feedback pulse train

$N$  = disk line density (pulses/cycle)

$f_{shaft}$  = speed of motor shaft (cycles/sec)

It should be noted, the encoded pulse train is actually position information. In order to determine the frequency of the motor shaft, a number of pulses over a period of time must be measured.

$$f_{tach} = \Delta \text{Pulse} / \Delta \text{time} \quad (\text{eqn 4.2})$$

$\Delta \text{Pulse}$  = change in pulses (count)

Substituting equation 4.2 in equation 4.1

$$\Delta \text{Pulse} / \Delta \text{time} = N f_{shaft}$$

taking the limit  $t \rightarrow 0$

$$\lim_{t \rightarrow 0} \Delta \text{Pulse} / \Delta \text{time} = d\text{Pulse}/dt = N f_{shaft} \quad (\text{eqn 4.3})$$

integrating both sides with respect to time

$$\text{Pulse} = N \int f_{shaft} dt + C \quad (\text{eqn 4.4})$$

Taking equation 4.4, the pulse train is N times the integral of shaft frequency. The integral of shaft frequency is shaft position, therefore the pulse train is N times shaft position with the constant of integrating C being the number of past pulses. The optical encoder is an implied integrator with gain N.

The optical encoder, used as a velocity sensor, is superior to the generator type tachometer for a fundamental reason. It has fewer moving parts. Additionally, its output is not subject to variations due to variations in air gap, temperature, and magnetic strength. Over a period of time the velocity feedback provided by a properly mounted optical encoder will not "drift."

## V. PLL SYSTEM DESIGN AND COMPUTER MODEL SIMULATION

The nonlinear nature of the digital phase-locked loop scheme suggested in Chapter 3 makes an exact analytical design procedure very difficult. A simplified approach is to make a linearized approximation of the system, then using computer simulation to determine the values for the control parameters to achieve the desired response.

A block diagram for the phase-locked loop scheme, using a logic controlled count enable/disable synchronous up/down counter as a phase frequency detector, is shown in Figure 5.1. The parallel proportional control path has gain,  $K_p$ ,

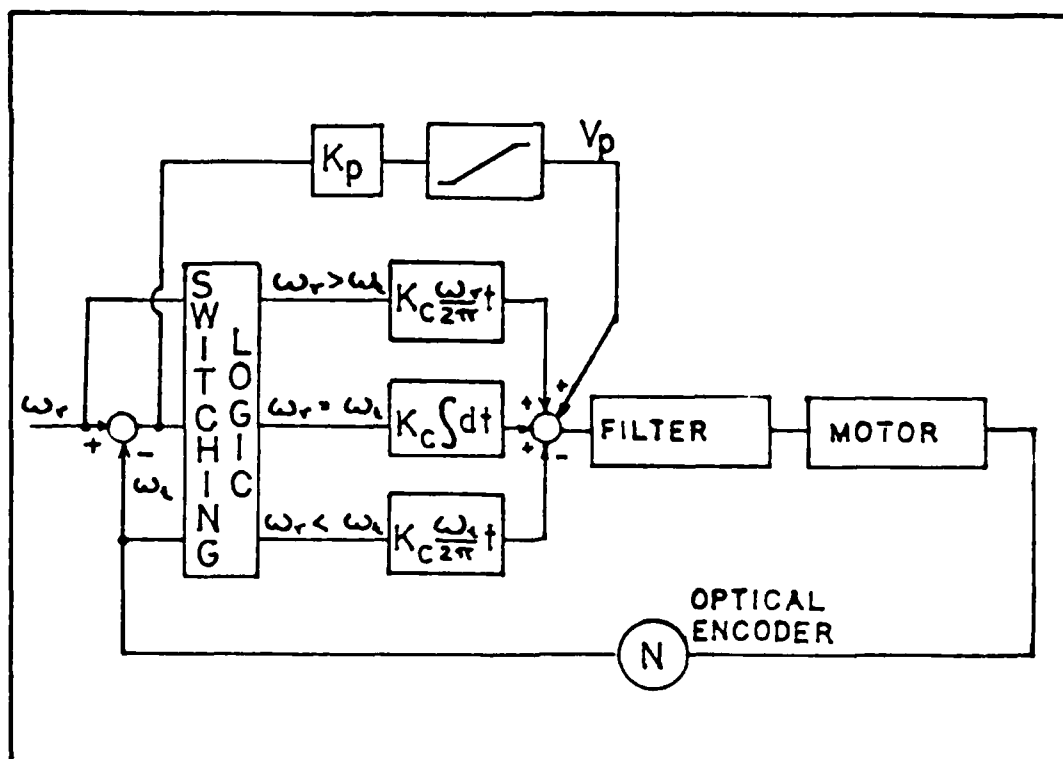


Fig. 5.1 Block Diagram of Digital PLL Control Scheme Indicating Nonlinear Elements

and a saturation nonlinearity. The saturating voltage levels of the proportional gain path play an important role in rapid system response and degree of overshoot to step inputs.

The interaction between the proportional control path and the up/down counter PFD will be examined along with the filter and optical encoder parameters in the following sections. First, however, the motor model will be presented.

#### A. BRUSHLESS D.C. MOTOR MODEL

The brushless d.c. motor is basically an open loop system. The phenomenon of back emf, however, serves as a "built-in" feedback loop which gives the system stability. A block diagram for the brushless d.c. motor is shown in Figure 5.2, illustrating the feedback effect of the back emf and the insertion of a torque loading [Ref. 8].

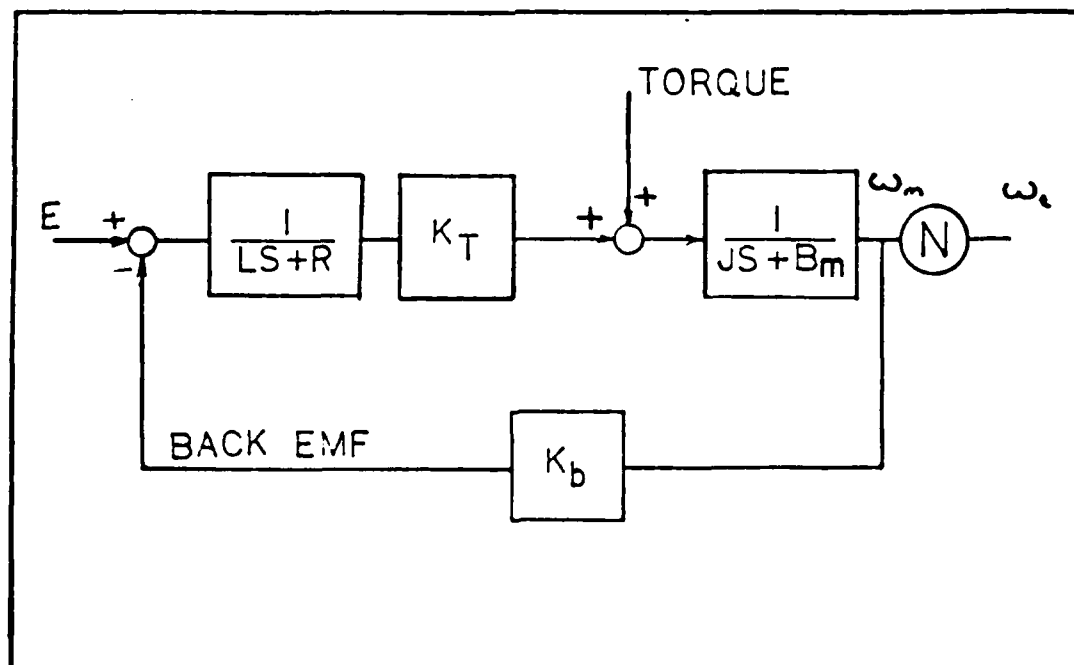


Fig. 5.2 D.C. Motor Block Diagram

The transfer function for an applied voltage is

$$\frac{\omega_m(s)}{E(s)} = \frac{K_T}{LJ s^2 + (LB_m + RJ) s + (RB_m + K_b K_T)} \quad (\text{eqn 5.1})$$

and the tachometer velocity  $\omega_t$  is

$$\omega_t = N \omega_m \quad (\text{eqn 5.2})$$

where  $N$  is the optical encoder line density.

A listing of typical parameters for a brushless d.c. motor is provided in Table I. These are the motor parameters used in the system design and simulation.

TABLE I  
TYPICAL MOTOR PARAMETERS

Stator inductance	$L$	0.0016 Henry
Stator resistance	$R$	2.74 ohms
Torque constant	$K_T$	15.9 oz-in/amp
Back emf constant	$K_b$	0.112 volt/(rad/sec)
Rotor inertia	$J_m$	0.001 oz-in/(rad/sec <sup>2</sup> )
Optical encoder disk inertia	$J_o$	0.002 oz-in/(rad/sec <sup>2</sup> )
Total motor inertia	$J$	0.003 oz-in/(rad/sec <sup>2</sup> )
Viscous friction coefficient	$B_m$	0.0015 oz-in/(rad/sec)

Equation 5.1 in factored form, assuming  $R B_m$  to be negligible compared to  $K_t K_b$

$$\frac{\omega_t(s)}{\omega_r(s)} = \frac{1/K_b}{(\tau_1 s + 1)(\tau_2 s + 1)} \quad (\text{eqn 5.3})$$

where  $\tau_1 = -1/p_1$  ;  $\tau_2 = -1/p_2$

with  $P_1$  and  $P_2$  being the roots of the characteristic equation

$$LJS^2 + (LB_m + RJ)S + K_T K_b = 0 \quad (\text{eqn 5.4})$$

substituting the values from Table I into equation 5.4 yields

$$P_1 = -254 \quad P_2 = -1458$$

and the time constants

$$\tau_1 = 3.94\text{mS} \quad ; \quad \tau_2 = 685.9\mu\text{S}$$

The motor is a stable second order system with two real roots. For a given input voltage it will provide a constant speed. However, because the motor is an open loop system, it cannot provide for speed regulation in the presence of torque loading or disturbances. In order to provide speed regulation, the phase-locked loop is included as a method of speed control.

#### B. DIGITAL PHASE FREQUENCY DETECTOR

The block labeled switching logic in Figure 5.1 is the up/down counter's enable/disable logic as discussed in Chapter 3. The output of the switching logic shows three paths, which are the modes available to the up/down counter, namely:

1.  $\omega_r > \omega_t$  , down count disabled
2.  $\omega_r < \omega_t$  , up count disabled
3.  $\omega_r = \omega_t$  , up/down count possible

In modes 1 and 2 the system is not phase-locked and the up/down counter acts as a variable voltage in a path parallel

and added to the proportional control voltage. The rate at which the up/down counter varies depends on which logic mode it is in and whether the "driving" signal is a constant or variable frequency.

As an example, let  $\omega_r > \omega_k$  and  $\omega_r$  is constant. That is, a constant motor speed is desired and the motor is under speed. The proportional control path, from the frequency-to-voltage converters through the differential amplifier in Figure 3.3, will provide a voltage ( $V_p$ ) that is proportional to the difference between the reference speed ( $\omega_r$ ) and the feedback speed ( $\omega_k$ ), within the saturation limits of the amplifier.

$$V_p = K_p (\omega_r - \omega_k)$$

The up/down counter will count up (down count disabled) at a rate proportional to  $\omega_r$ . With  $\omega_r$  being constant, the up/down counter output voltage ( $V_c$ ) will be

$$V_c(t) = K_c k u(kT) \text{ for } kT \leq t < kT+T \quad (\text{eqn 5.5})$$

where  $K_c$  = voltage increment/count

$$T = 2\pi/\omega_r \text{ sec/count}$$

$$t = \text{time (sec)}$$

$$k = \text{integer value of count}$$

$$u(kT) = \text{unit step function}$$

From equation 5.5 the time required for the up/down counter to reach an operating voltage sufficient to drive the motor at the reference speed is a function of  $K_c$  and  $\omega_r$ .



Now consider the case when  $\omega_i > \omega_r$ . The motor is over speed and the counter will only count down (count up is disabled). The rate at which it will count down is proportional to  $\omega_i$ . Initially,  $\omega_i$  is greater than  $\omega_r$  and slows until  $\omega_i = \omega_r$ , which means the rate at which the counter changes also slows, but not less than  $\omega_r$ . The counter will count down faster than it counts up.

The third mode which can exist is when the reference speed and feedback speed are very nearly equal. In this case, the system is phase-locked, the up/down counter is acting as a frequency error integrator, and the proportional control signal is nearly zero. Under these conditions the digital phase frequency detector can be modeled as a proportional-integral controller as shown in Figure 5.3 (see equation 3.6).

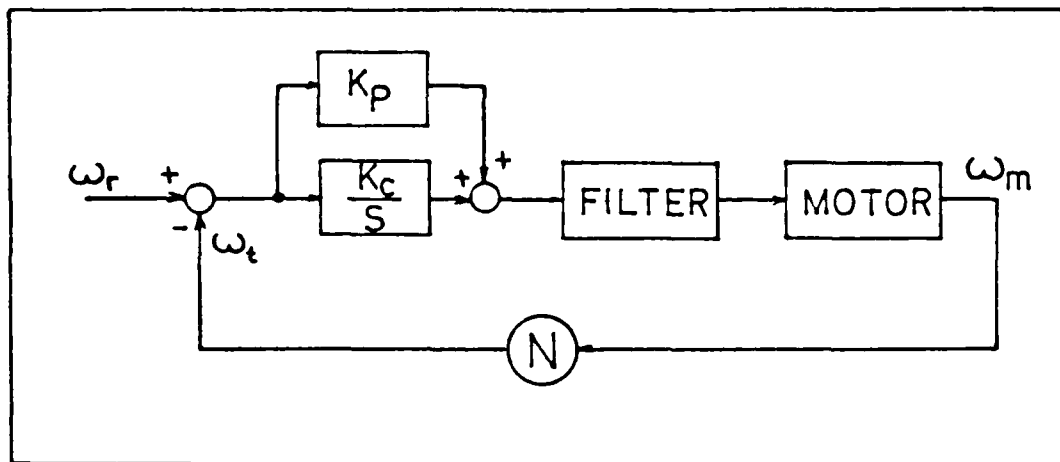


Fig. 5.3 Block Diagram of Digital PFD in Phase-Lock

The block diagram in Figure 5.3 is only an approximation of the PLL scheme when the system is in phase-lock. It

should be kept in mind, when choosing the system parameters, the system does operate in three modes.

### C. PLL DESIGN PARAMETERS

The choice of system parameters depends on the system application. There are clearly trade offs to be made. This section will discuss how each parameter affects the system's response.

#### 1. Incremental Counter Voltage $K_c$

The value of  $K_c$  is the limiting factor in the dynamic range of control. It also affects the resolution of the frequency error integration and rate at which the up/down counter can change voltage. The rate at which the counter changes is equally affected by  $N$ , the optical encoder line density.

The minimum value of  $K_c$  is specified by the size of the counter (number of bits) and the range of motor speed the counter must track.

$$K_c(\min) = V_{\text{range}} / \text{Count}_{\text{max}} \quad (\text{eqn 5.6})$$

where  $V_{\text{range}}$  = voltage range required to drive the motor over the desired speed range

$\text{Count}_{\text{max}}$  = maximum count available in the counter

For example, it is desired to control the motor speed over a range of 0 to 1000 rad/sec. The voltage required to drive the motor at 1000 rad/sec is 112 volts. Assume an

8-bit counter, the maximum count then is  $2^8 = 256$  which includes 0. So the maximum count available is 255 then

$$K_C(\text{min}) = 112 \text{ volts}/255 \text{ counts} = 0.439 \text{ volts/count} \quad (\text{eqn 5.7})$$

With this value of  $K_C$  the controller could drive the motor at 1000 rad/sec assuming no torque loading or other disturbance. If a torque load is expected at the maximum speed of operation,  $K_C$  must be increased to avoid exceeding the counter's limit. Exceeding the counter's limit must be avoided, most up/down counters cycle to zero when their maximum count is exceeded.

Figures 5.4 through 5.7 illustrate the effect on frequency error integration resolution and time required to achieve phase-lock for two different values of  $K_C$  (all other system parameters being the same). In Figure 5.4, with  $K_C = 3.30$ , it takes 5.25 ms for the counter to reach  $V_n$  (see Figure 3.2 and equation 3.7). The largest percent error variation from the reference speed is 0.0537% in Figure 5.5 once phase-lock is acquired. In Figure 5.6, with  $K_C = 1.32$ , it takes 14.0 ms for the counter to reach  $V_n$ . However, the percent error variation from the reference speed is only 0.0186% in Figure 5.7. Clearly, the larger value of  $K_C$  has the advantage of acquiring phase-lock much quicker at the expense of speed regulation error.

## 2. Optical Encoder Line Density N

The rate at which the counter counts up and down is directly affected by the optical encoder line density. From

# PLL MOTOR SPEED CONTROL SPEED AND DAC VOLTS

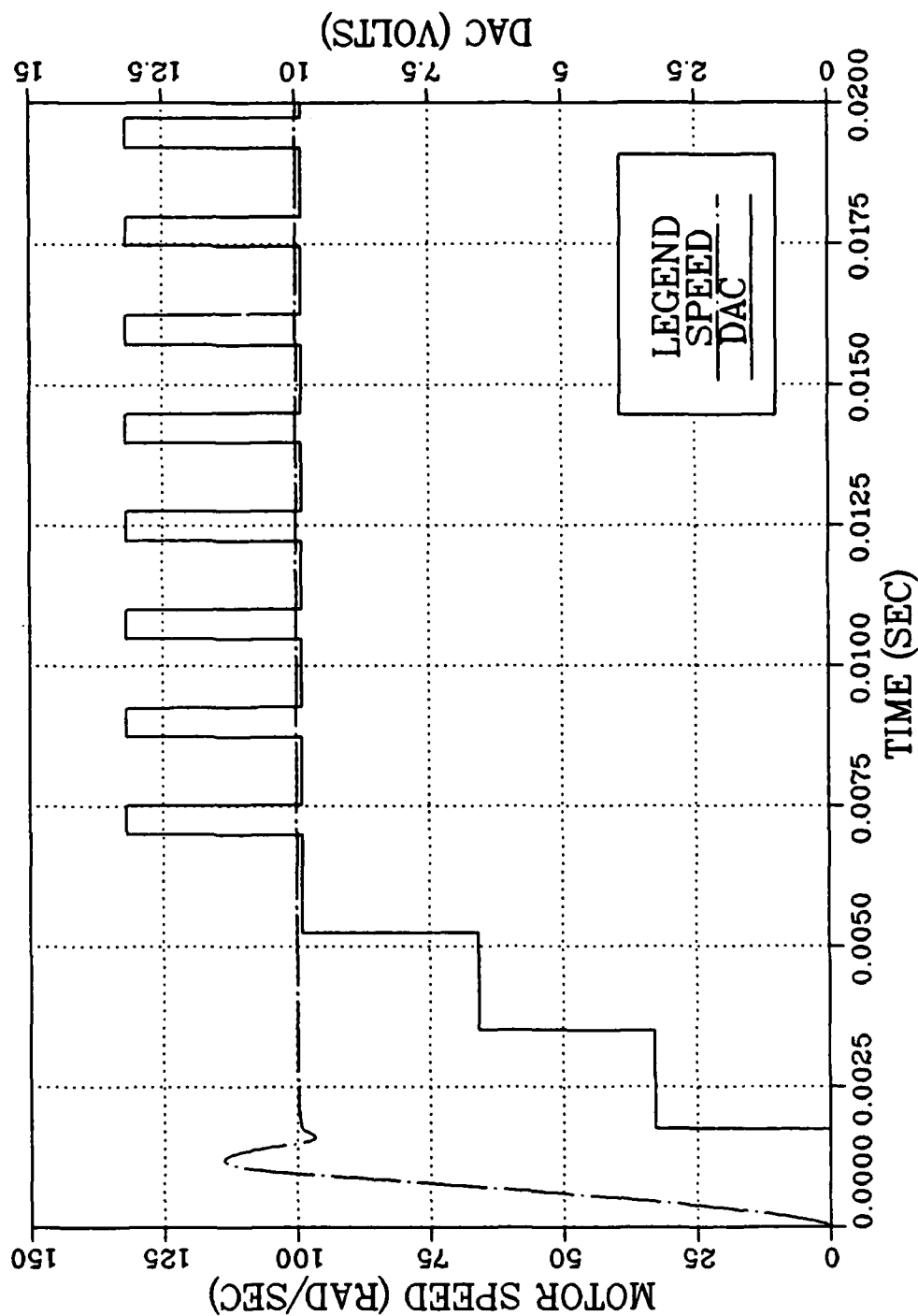


Fig. 5.4  $K_c = 3.30$ ,  $K_p = 1.32$ ,  $N = 36$   $Z_f = 5000$

$P_f = 50,000$

# PLL MOTOR SPEED CONTROL ERROR AND VP

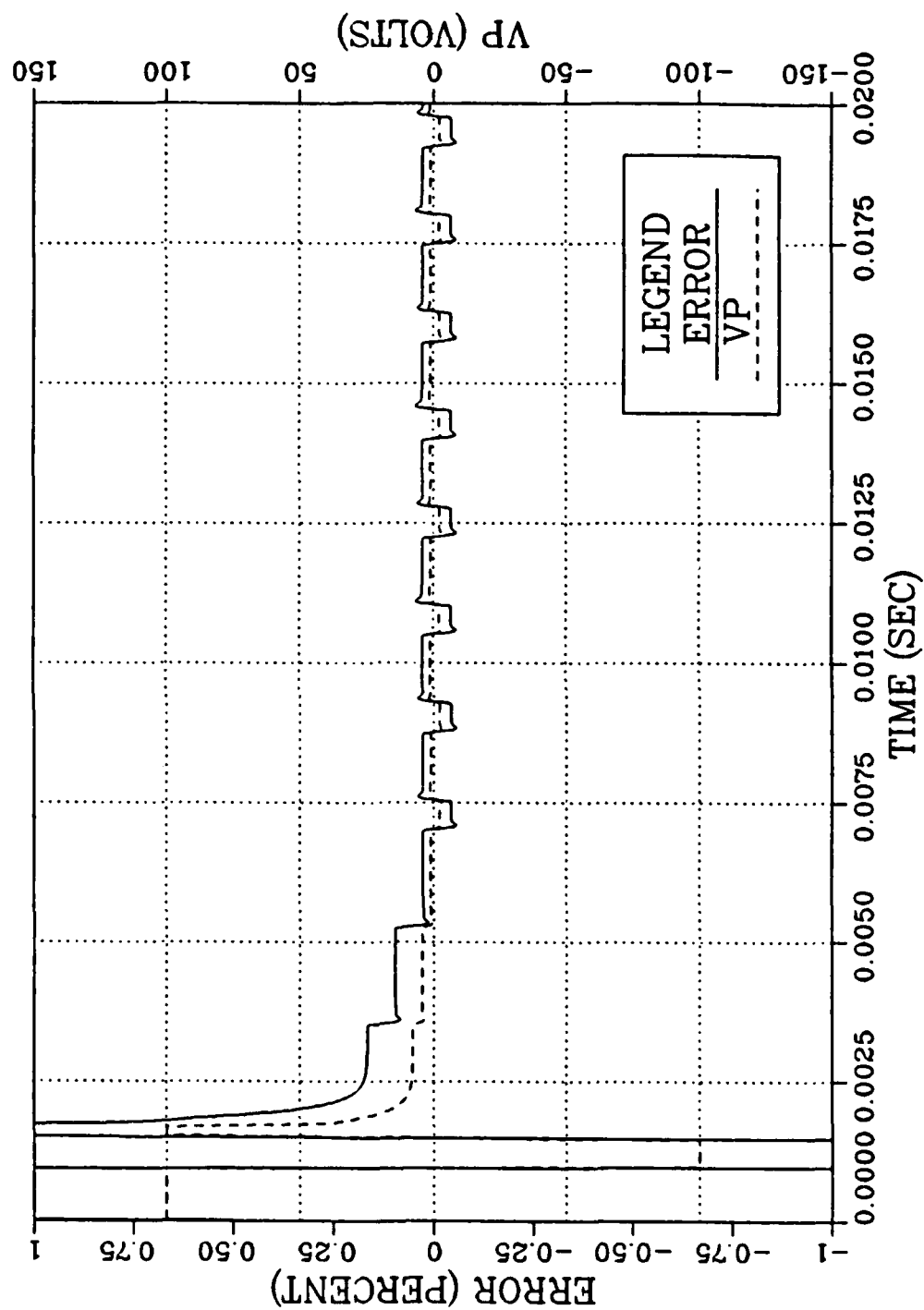
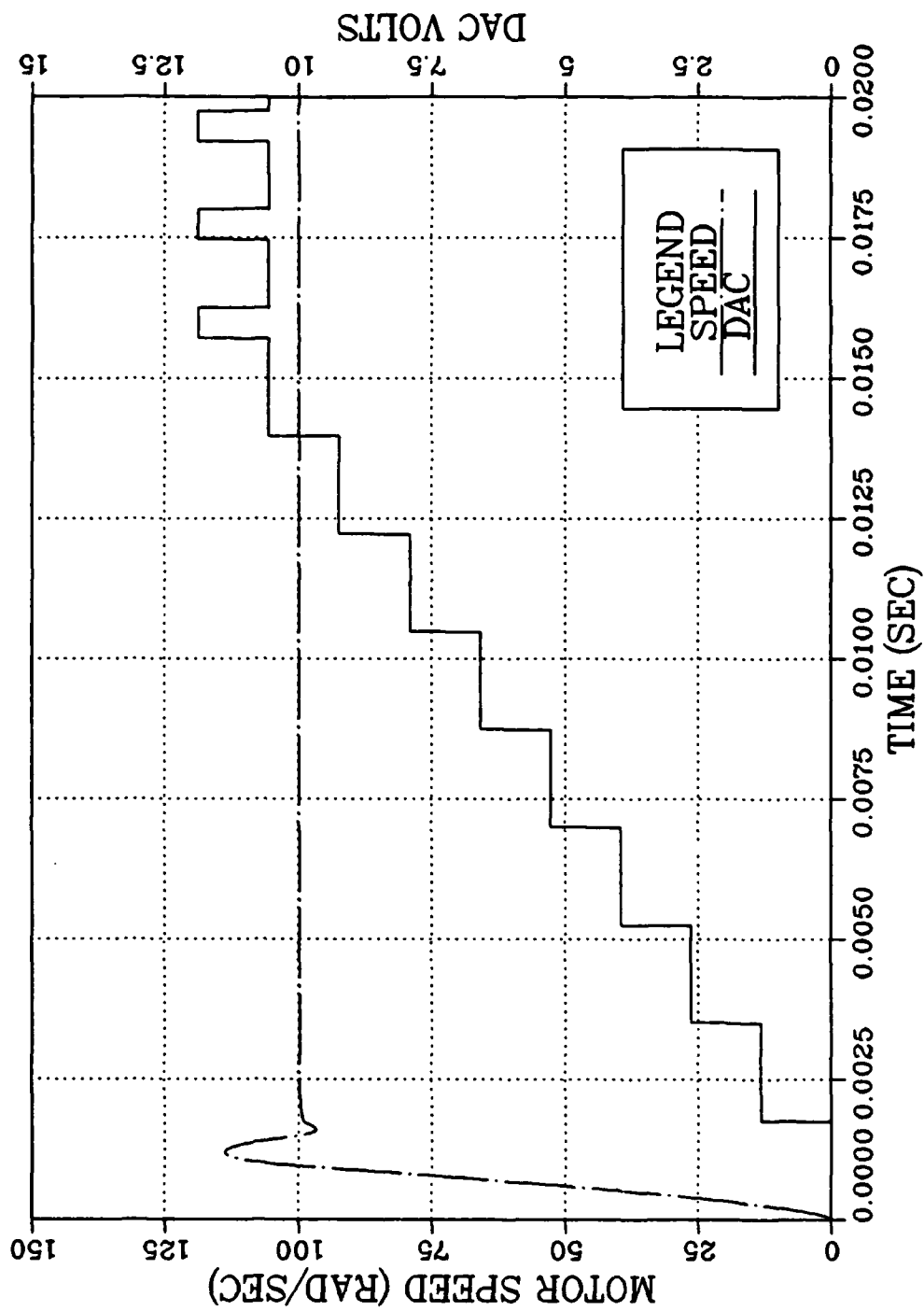


Fig. 5.5  $K_c = 3.30$ ,  $K_p = 1.32$ ,  $N = 36$ ,  $Z_f = 5000$   
 $P_f = 50,000$

# PLL MOTOR SPEED CONTROL SPEED AND DAC VOLTS



# PLL MOTOR SPEED CONTROL ERROR AND VP

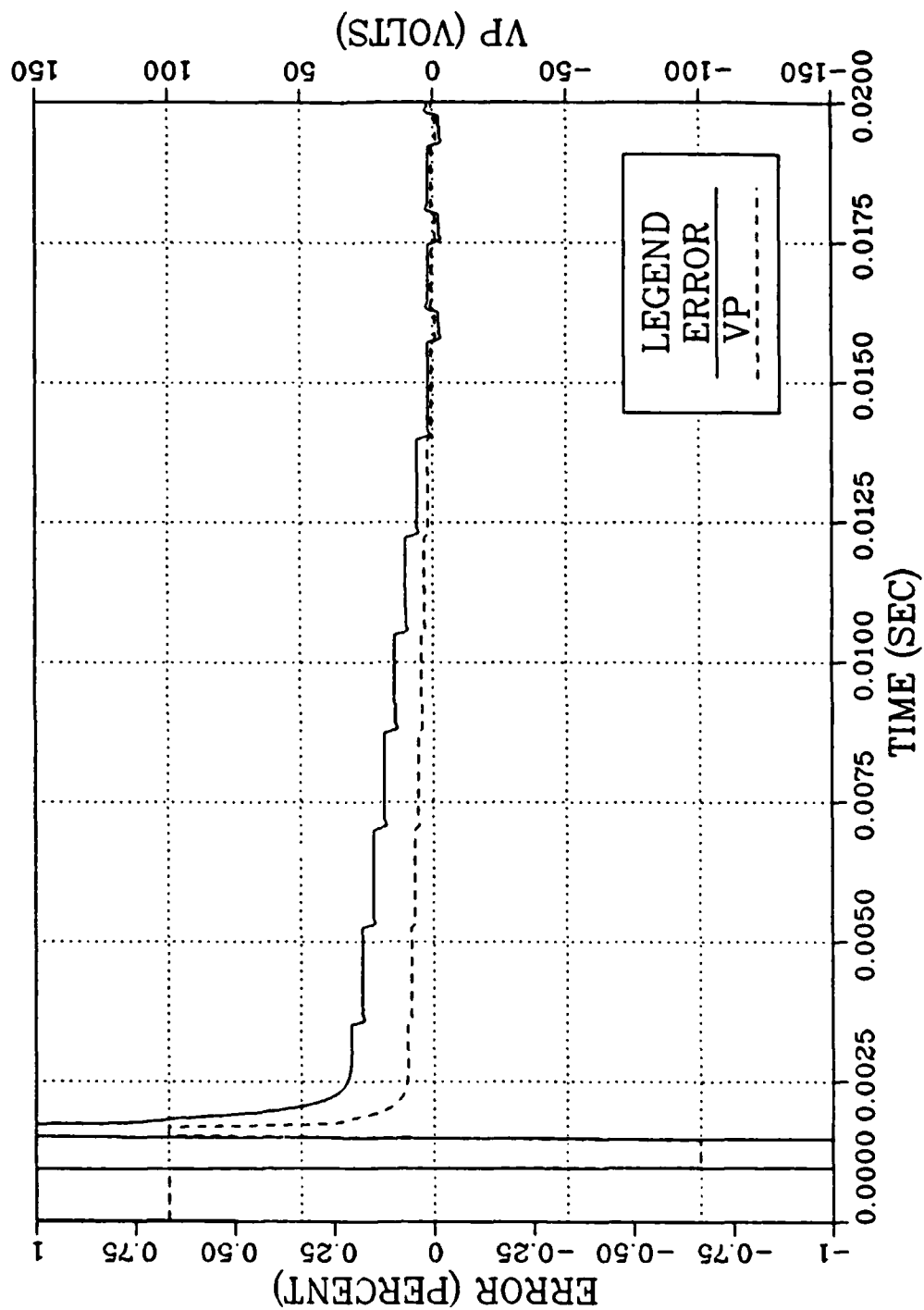


Fig. 5.7  $K_c = 1.32$ ,  $K_p = 1.32$ ,  $N = 36$ ,  $Z_f = 5000$   
 $P_f = 50,000$ ,  $\omega_d = 100.0$

equation 4.1 the optical encoder acts as an amplifier and is so represented in the system block diagram (Figure 5.1). The counter is triggered by the leading edges from reference frequency pulse train and feedback pulse train which are  $N$  times the desired motor frequency and  $N$  times the motor frequency respectively. By increasing  $N$ , the rate at which the counter will change also increases.

Figures 5.8 and 5.9 illustrate the effect of increasing  $N$  from 36 (in Figures 5.6 and 5.7) to 120. In Figure 5.8 the system acquires phase-lock in 6.30 ms as compared to 14.0 ms with  $N = 36$ . The speed error is further reduced to less than 0.008 percent by increasing  $N$ .

From the discussion of optical encoders, Chapter 4, it is evident that the position of the motor is "sampled" every  $1/N$  revolution. The value of  $N$  then is a measure of the sampling rate of the system which, in part, explains the reduced speed error with increased  $N$ . There is a limit to increasing the value of  $N$ . As previously mentioned,  $N$  is a gain element and as such increasing  $N$  will tend to make the system unstable.

### 3. Proportional Gain $K_p$ and Saturation Amplifier

The proportional control voltage ( $V_p$ ) plays an important role in the system response to step inputs of both reference frequency and torque.



# PLL MOTOR SPEED CONTROL SPEED AND DAC VOLTS

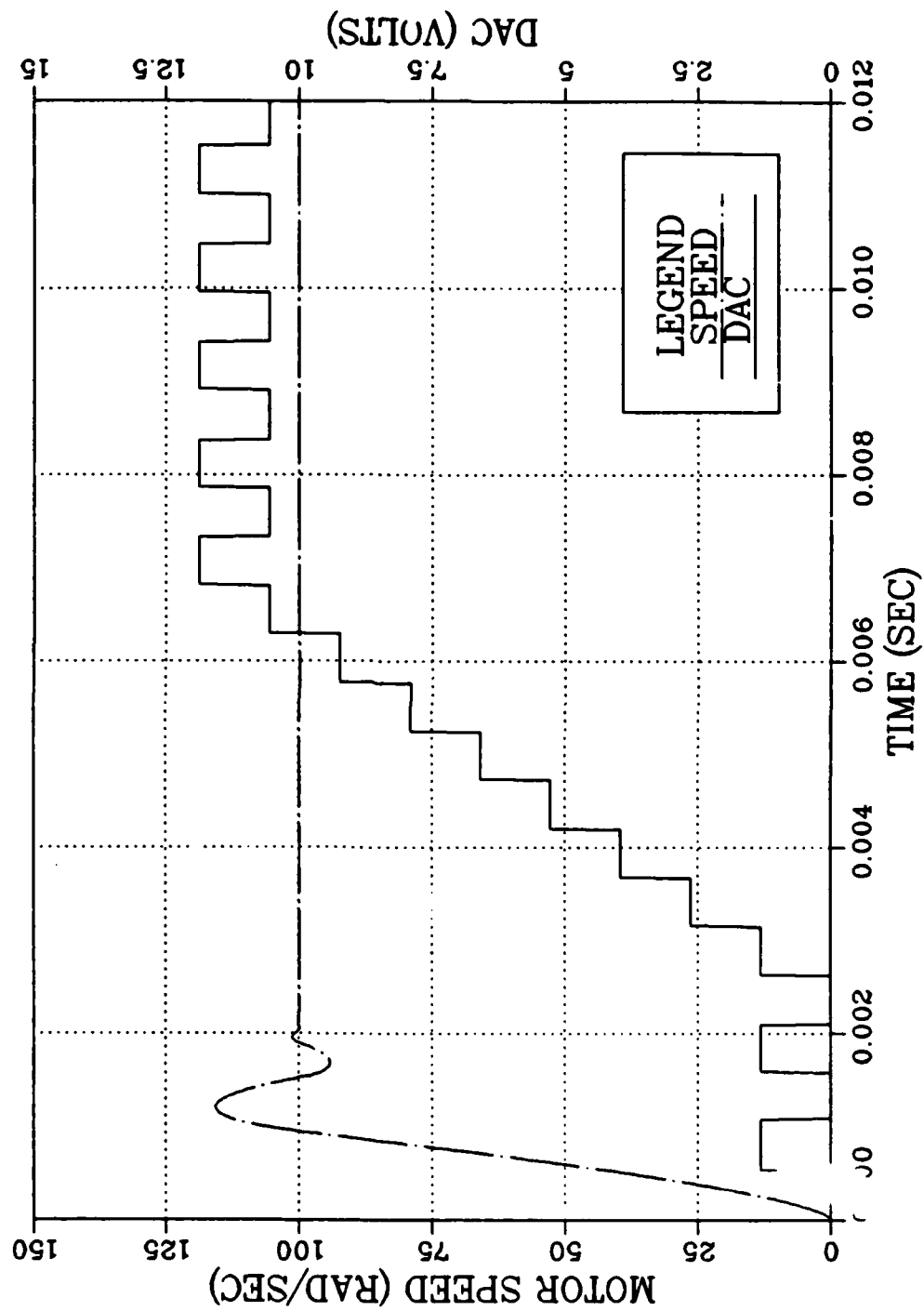


Fig. 5.8  $K_p = 1.32$ ,  $K_c = 1.32$ ,  $N = 120$ ,  $Z_f = 5000$

$P_f = 50,000$

# PLL MOTOR SPEED CONTROL ERROR AND VP

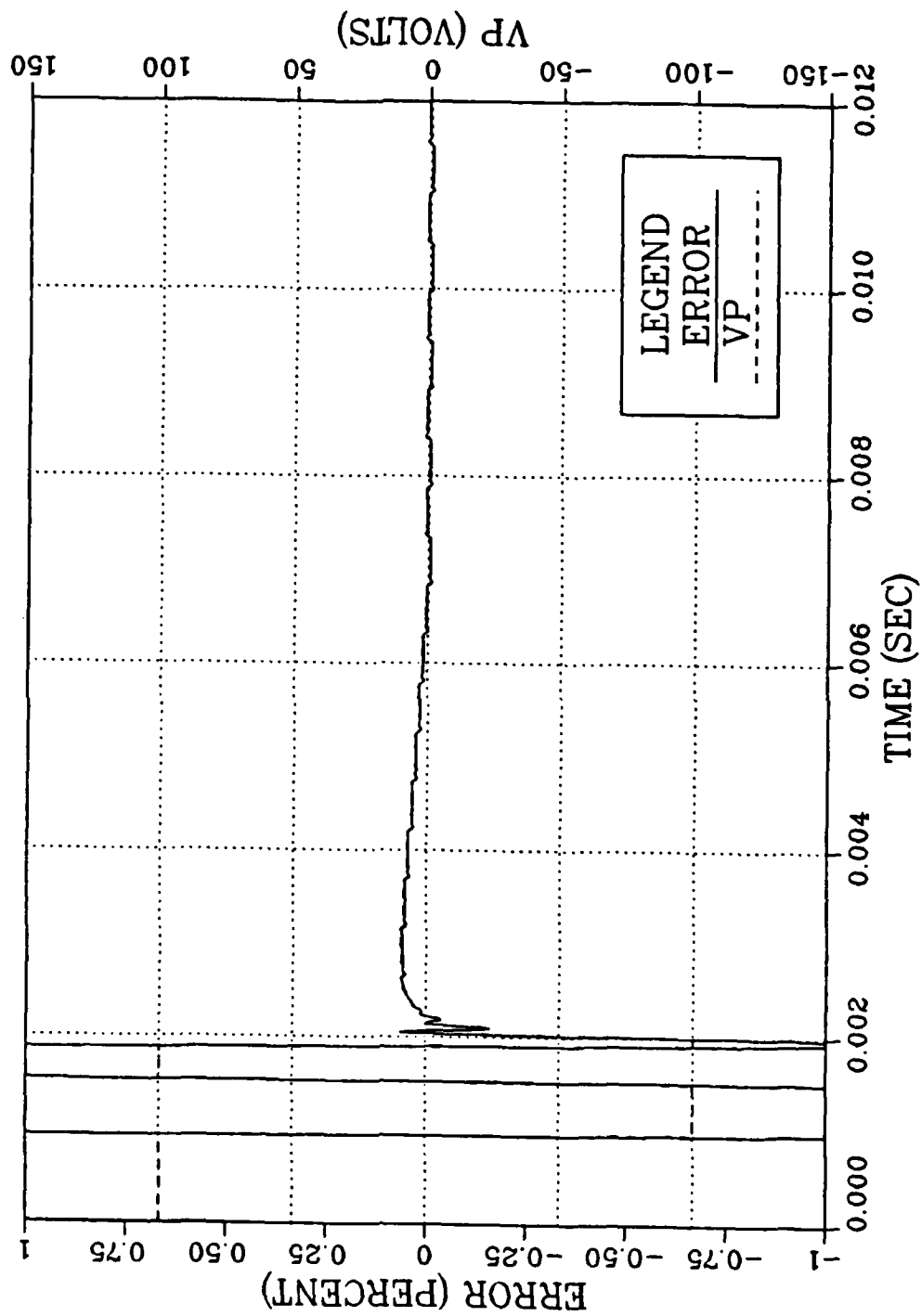


Fig. 5.9  $K_p = 1.32$ ,  $K_c = 1.32$ ,  $N = 120$ ,  $Z_f = 5000$   
 $P_f = 50,000$

From the block diagram, Figure 5.1

$$\begin{aligned} V_p &= K_p \cdot \omega_e \quad \text{if } |V_p| \leq V_{\text{sat}} \\ &= \pm V_{\text{sat}} \quad \text{if } |V_p| > V_{\text{sat}} \end{aligned} \quad (\text{eqn 5.8})$$

where  $V_{\text{sat}}$  = Amplifier saturation voltage  
and

$$\omega_e = (\omega_r - \omega_i) \quad (\text{eqn 5.9})$$

with  $\omega_r = N \cdot \text{desired speed } (\omega_d)$

$\omega_i = N \cdot \text{motor speed } (\omega_m)$

then

$$\omega_e = N \cdot (\omega_d - \omega_m) \quad (\text{eqn 5.10})$$

Substituting equation 5.10 in 5.8 yields

$$V_p = K_p N (\omega_d - \omega_m) \quad (\text{eqn 5.11})$$

from equation 5.11  $V_p$  is a function of both  $K_p$  and  $N$ . Clearly, if both  $K_p$  and  $N$  are chosen to be large, then the proportional control voltage,  $V_p$ , would be large for even small speed errors.

The amplifier used for the proportional control voltage, to be practical, must have saturation limits ( $\pm V_{\text{sat}}$ ). In order for the proportional control signal to operate in the linear region of the amplifier, the gain  $K_p N$  must not be so large as to drive the amplifier into saturation for small speed errors when the system is in phase-lock.

The magnitude of the saturation voltage must also be considered in the system design. A large saturation voltage provides a fast response for large step speed command inputs;

however, it causes an overshoot for smaller speed command inputs. An example of the system response to two speed commands using two different values for  $V_{sat}$  is shown in Figures 5.10 through 5.13. In Figure 5.10 with  $V_{sat} = 50$  volts and  $\omega_d = 100$  rad/sec, there is a 6% overshoot, with phase-lock acquired in 5.25 ms and a steady state error of less than 0.008 %, which is the same in Figure 5.11 except  $V_{sat} = 100$  volts and there is a 15% overshoot. In Figure 5.12 with  $V_{sat} = 50$  volts and  $\omega_d = 1000$ , there is a 5% overshoot with phase-lock acquired in 10.2 ms. In Figure 5.13 with  $V_{sat} = 100$  volts, there is a 2% overshoot but phase-lock is acquired in only 7.75 ms. Both have steady state errors of 0.0008% but with  $V_{sat} = 100$  volts, phase-lock is acquired in less time.

#### 4. Filter

In developing a design approach for the system filter, two characteristics become clear from simulation studies:

1. A low pass filter induced an unacceptable limit cycle.
2. In order for the up/down counter to achieve a true phase-lock, with a high reference frequency input, the bandwidth of the linearized phase-lock model had to be sufficiently wide.

Justification for the above statements is provided in the next section where the simulation studies are presented.

# PLL MOTOR SPEED CONTROL SPEED AND DAC VOLTS

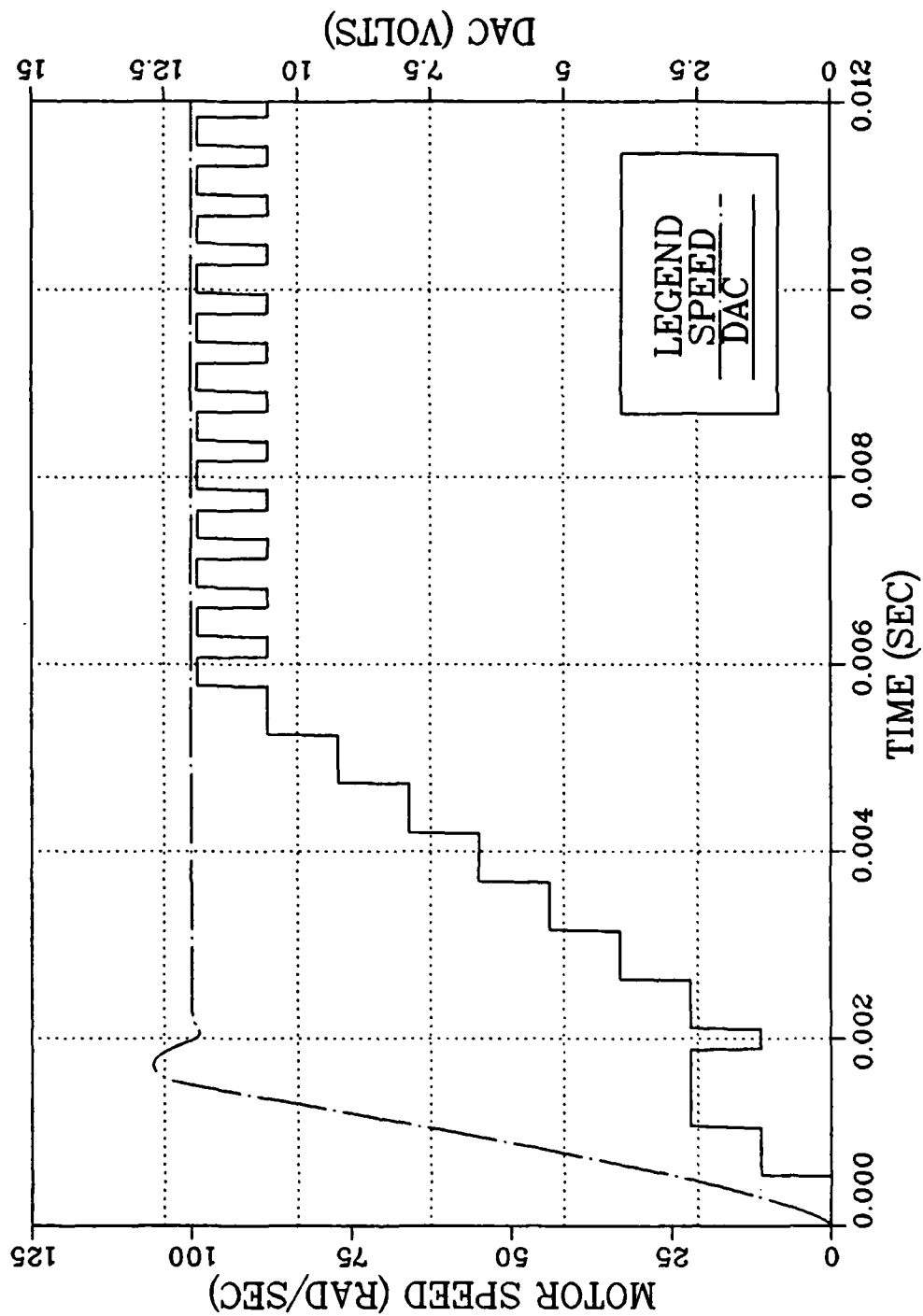


Fig. 5.10  $K_c = 1.32$ ,  $K_p = 1.32$ ,  $N = 120$ ,  $Z_f = 5000$   
 $P_f = 50,000$   $V_{sat} = 50.0$   $\omega_d = 100.0$

# PLL MOTOR SPEED CONTROL SPEED AND DAC VOLTS

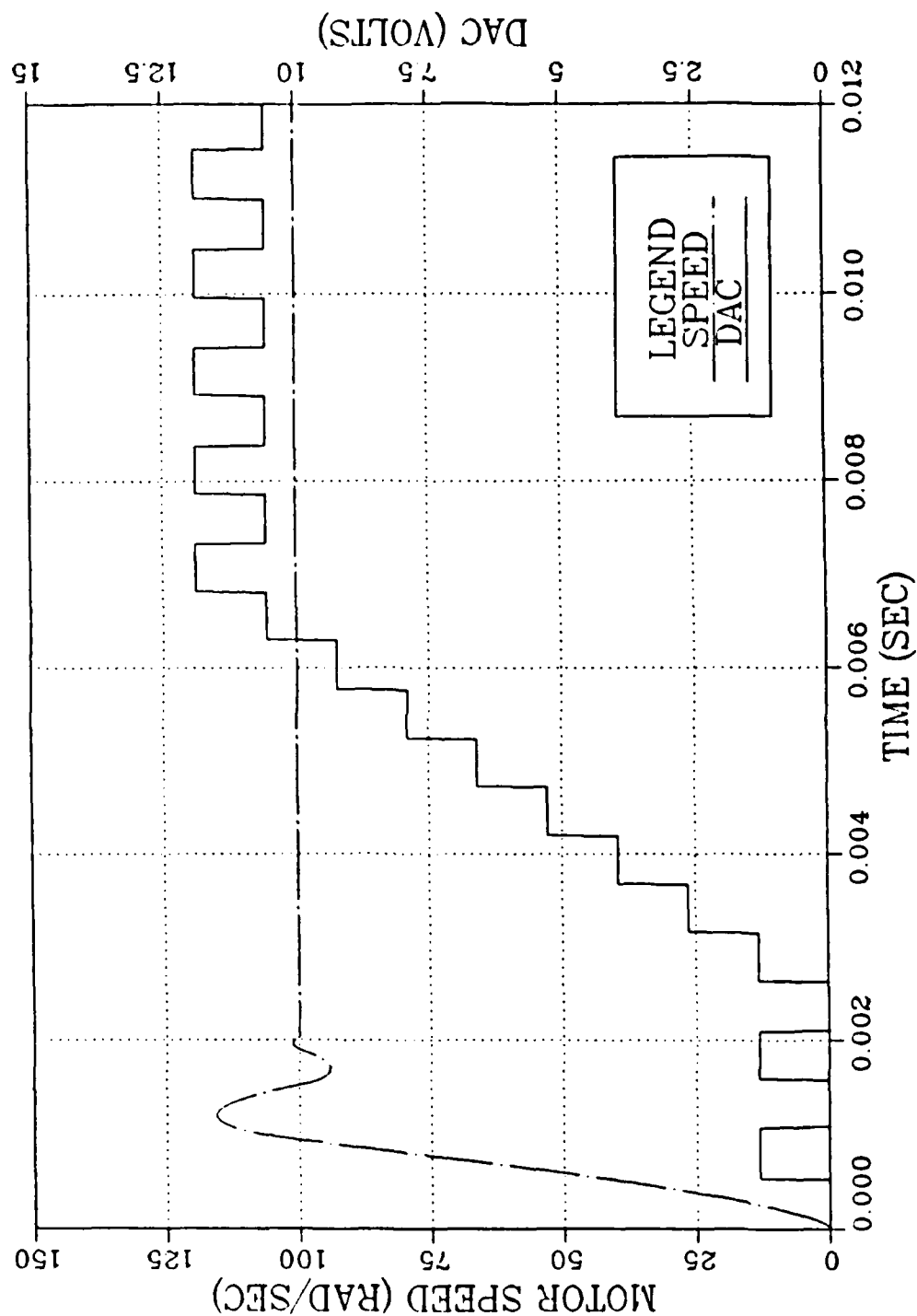


Fig. 5.11  $K_c = 1.32$ ,  $K_p = 1.32$ ,  $N = 120$ ,  $Z_f = 5000$   
 $P_f = 50,000$   $V_{sat} = 100.0$   $\omega_p = 100.0$

# PLL MOTOR SPEED CONTROL SPEED AND DAC VOLTS

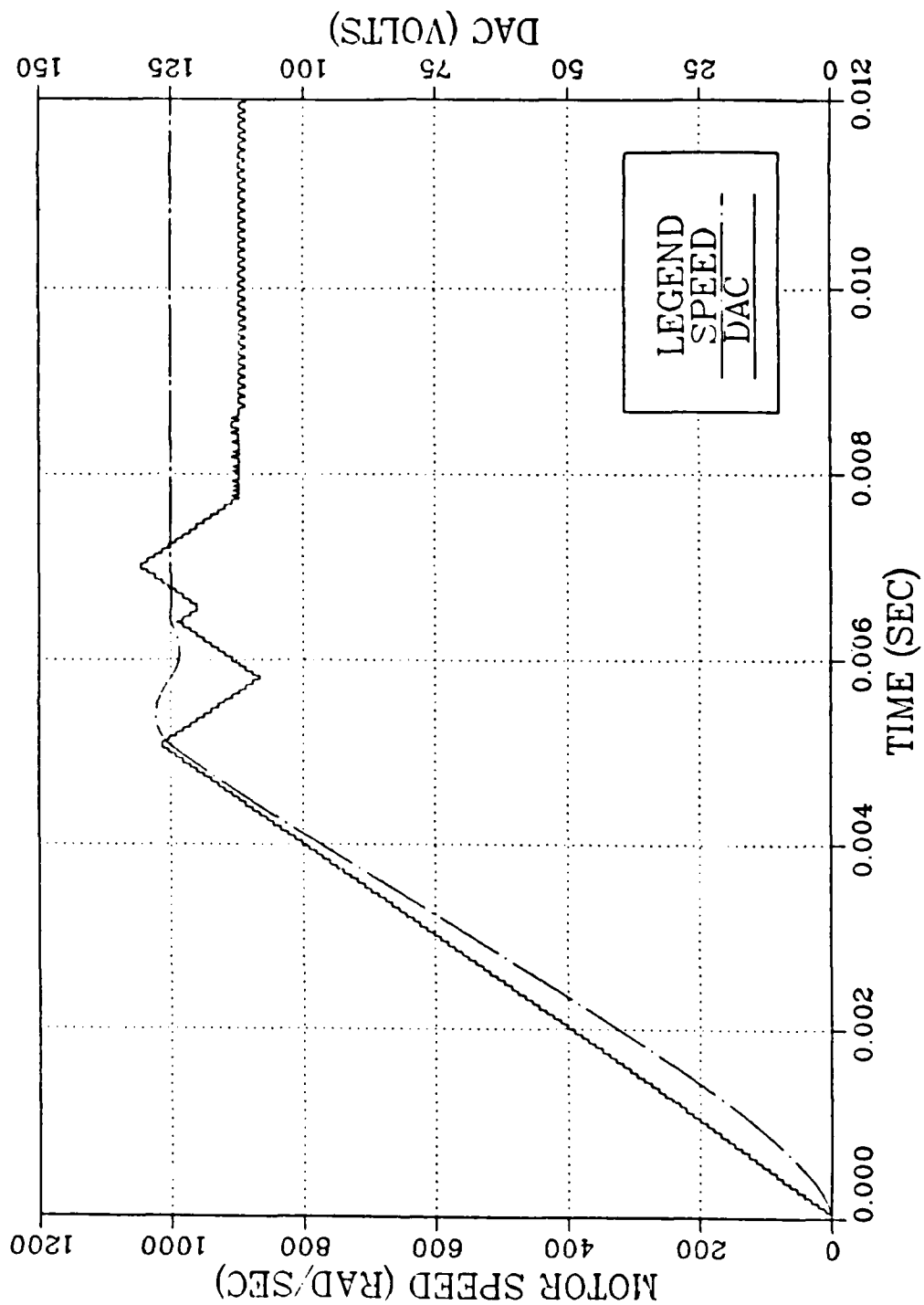


Fig. 5.12  $K_c = 1.32$ ,  $K_d = 1.32$ ,  $N = 120$ ,  $Z_f = 5000$   
 $P_f = 50,000$   $V_{sat} = 50.0$   $\omega_d = 1000$

# PLL MOTOR SPEED CONTROL SPEED AND DAC VOLTS

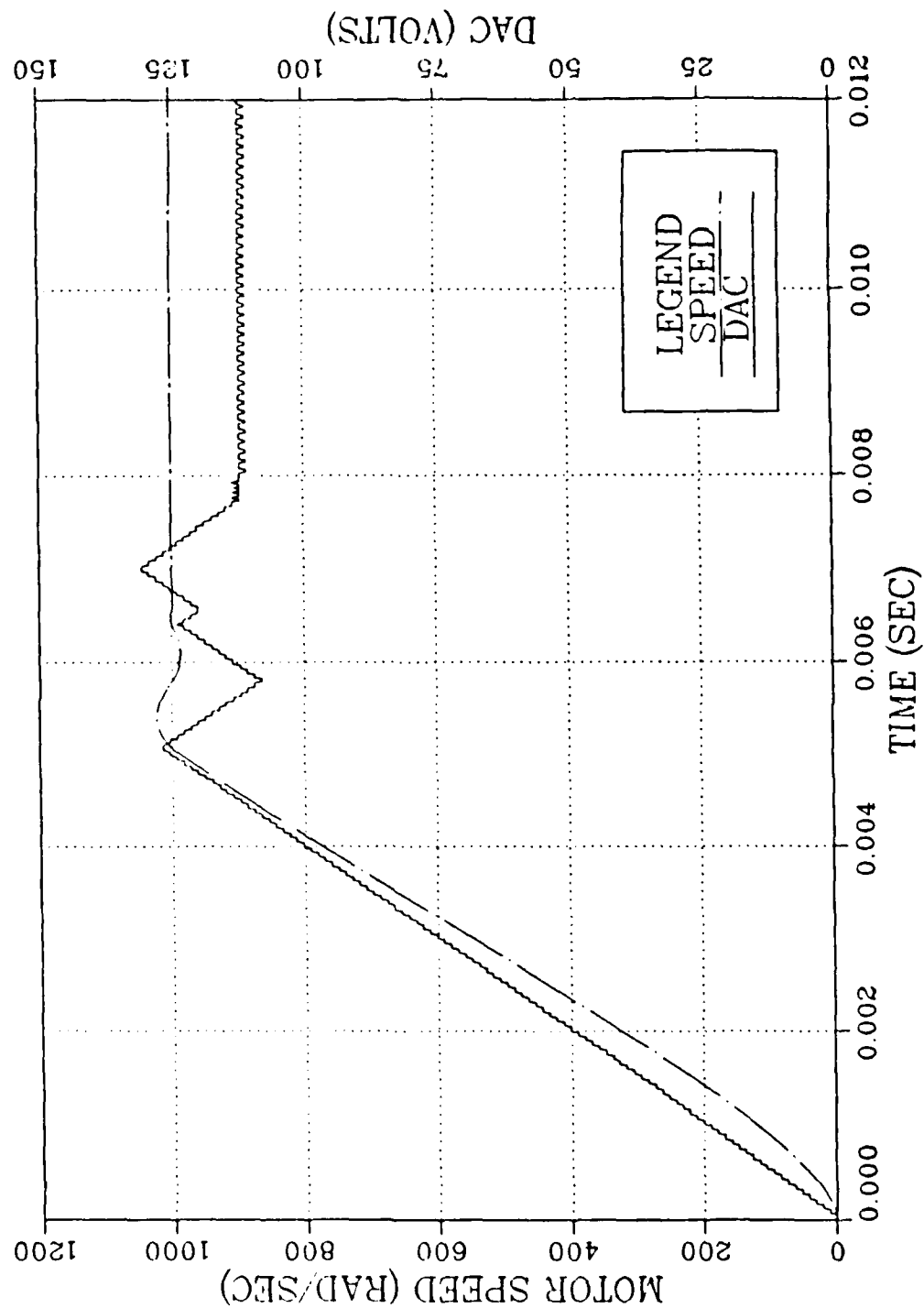


Fig. 5.12  $K_c = 1.32$ ,  $K_d = 1.32$ ,  $N = 120$ ,  $Z_f = 5000$   
 $P_f = 50,000$   $V_{sat} = 50.0$   $\omega_p = 1000$



#### D. SIMULATION STUDIES

When analyzing a linear system the Bode diagram, Nichol's plot and other classical methods can be used to determine the system's transient response and stability. If these methods are applied to nonlinear systems, often the best that can be expected is an estimate of the nature of the transient response. In order to obtain more accurate predictions, simulation studies are used [Ref. 9].

A computer simulation model of the digital PLL system shown in Figure 5.1 was developed using the IBM Digital Simulation Language (DSL/360). A listing of the basic program is provided in Appendix A.

Figure 5.1 illustrates the three modes of operation of the digital PLL scheme described in Chapter 3, using the up/down count enable/disable logic. Of primary importance to this thesis is the proper operation in the phase-locked mode.

The linearized model in Figure 5.3 is an approximation of the system when operating in the phase-locked mode. The transfer function for this model is

$$\frac{\omega_o(s)}{\omega_r(s)} = \left[ \frac{K_p S + K_c}{S} \right] \frac{P_f}{Z_f} \left[ \frac{S + Z_f}{S + P_f} \right] \cdot N \cdot \left[ \frac{K}{(\tau_1 S + 1)(\tau_2 S + 1)} \right] \quad (\text{eqn 5.12})$$

where  $K_p$  = proportional gain (volts/(rad/sec))

$K_c$  = Counter gain (volts/rad)

$Z_f$  = filter zero

$P_f$  = filter pole

$N$  = optical encoder line density (pulses/rad)

$$K = \text{motor gain} = (8.929 \text{ (rad/sec)/volt})$$

$$\tau_1 = 1/P_1 = 1/254 \text{ sec}$$

$$\tau_2 = 1/P_2 = 1/1458 \text{ sec}$$

The desired control system performance was to provide less than 0.5 percent speed error for a step or ramped reference speed over a range of 100 to 1000 rad/sec. Also to provide the same speed regulation with up to a 90 oz-in torque applied.

In order to drive the motor at 1000 rad/sec the input voltage must be

$$1000 \text{ (rad/sec)} / 8.929 \text{ (rad/sec)/volt} = 112.0 \text{ volts (eqn 5.13)}$$

Assuming an 8-bit counter and 8-bit DAC is used, the minimum value for  $K_C$  (assuming no torque is applied at the maximum speed) from equation 5.6

$$K_C = 112 \text{ volts} / 255 \text{ counts} = 0.439 \text{ volts/count (eqn 5.14)}$$

An initial value of  $K_C = 0.66 \text{ volts/count}$  was chosen in order to provide control for a torque load at maximum speed.

The optical encoder line density,  $N$ , was arbitrarily chosen to be 36.

In an initial attempt to facilitate a simplified design approach, the filter zero was chosen to cancel the low frequency pole of the motor. The filter pole was selected to be one decade larger than the filter zero to provide a low pass filter effect, that is to make the system bandwidth less than  $N \cdot 1000 \text{ rad/sec}$ . The initial saturation voltage of the

proportional control amplifier was chosen to be 10.0 volts, to avoid overshoot for a step input of 100 rad/sec, and a proportional gain  $K_p = 0.066$  was selected to insure a large linear region of operation.

From equation 5.12 it can be seen the proportional-integral (PI) controller has a zero at  $K_c/K_p$ , therefore a small value of  $K_p$  provides for a large zero and subsequently reduces the system bandwidth.

Simulation runs were conducted using the above system parameters and it was observed that although the system behaved as expected for motor speeds of 100 rad/sec, as the speed was increased the up/down counter no longer would achieve a true phase-lock. At the higher reference frequencies the up/down counter would begin to transition between three voltage levels as shown in Figure 5.14. By reducing the value of  $N$ , it was found that the system would behave as expected at the higher motor speeds, however, the steady state error was significantly increased for lower speeds due to the reduced sampling rate. In an attempt to reduce the steady state speed error, the proportional gain was increased. It was observed that the reference frequency could now be increased before the system began the transition between three voltage levels.

By increasing  $K_p$ , the zero of the PI controller is moved to a lower value and the system bandwidth is increased. Figure 5.15 is the Bode plot of system with the initial parameters. Figure 5.16 shows the increased bandwidth of the

# PLL DAC PULSE TRAIN S1 AND S2 UNIT PULSE

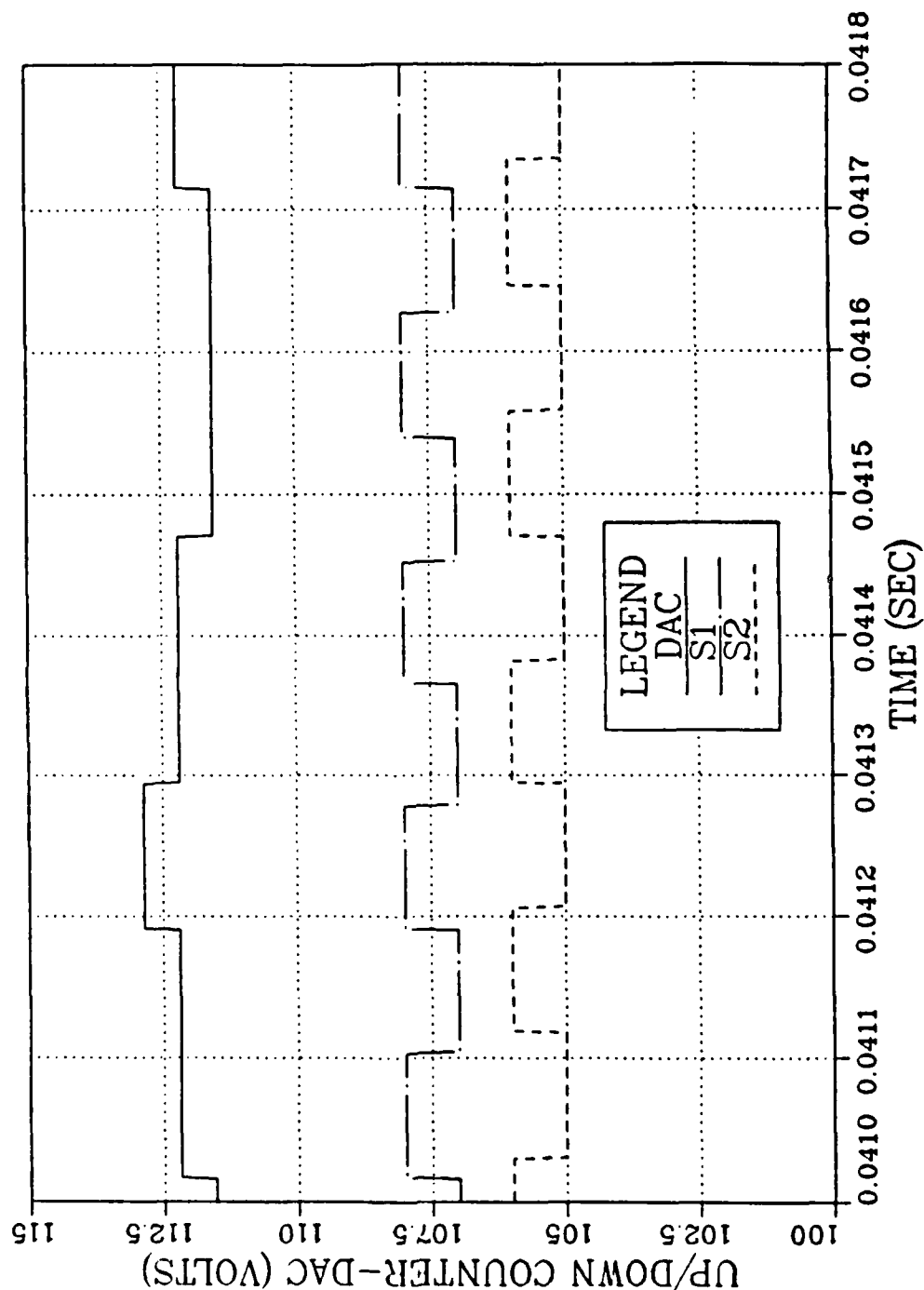


Fig. 5.14  $K_c = 0.66$ ,  $K_p = 0.066$ ,  $N = 36$ ,  $Z_f = 254$   
 $P_f = 2540$

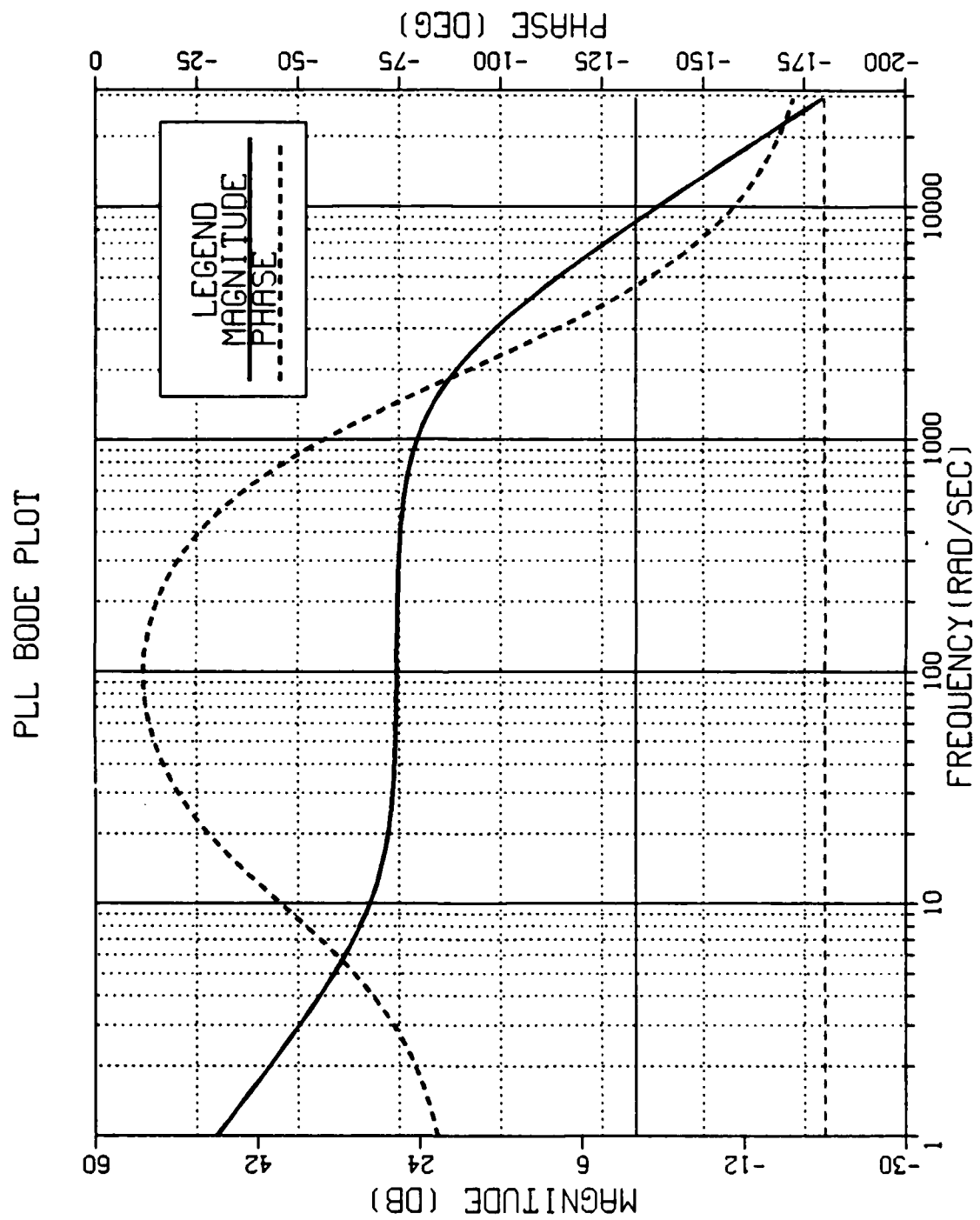


Fig. 5.15  $K_c = 0.66$ ,  $K_p = 0.066$ ,  $N = 36$ ,  $Z_f = 254$ ,  $P_f = 2540$

system with  $K_p$  increased to 0.66. The output of the up/down counter for the motor speed of 1000 rad/sec is shown in Figure 5.17. Clearly, there is a cycle for cycle correspondence between the input pulse train  $S_1$  and the feedback pulse train  $S_2$ . The output of the up/down counter is a pulse train of constant frequency and pulse width, with an average value sufficient to drive the motor at the reference speed.

Further simulation runs were conducted with  $K_p = 0.66$  and increased values of  $N$ . The results were that the steady state output of the up/down counter began to exhibit the transition between three voltage levels again. With the successful results of extending the bandwidth by moving the PI controller zero, the bandwidth was increased by changing the filter pole-zero combination. A Bode plot of the system with  $N = 72$  and a filter zero at 5000 rad/sec and pole at 50,000 rad/sec is shown in Figure 5.18. The steady state output of the up/down counter-DAC is shown in Figure 5.19, again by extending the bandwidth the optical encoder line density could be increased, from  $N = 36$  to  $N = 72$ , and the system would acquire phase-lock.

The objective is clearly to make  $N$  as large as practical. Increasing  $N$  has several beneficial effects, of particular benefit with the counter's enable/disable logic, increasing  $N$  increases the rate at which the counter will change. Increasing  $N$  also reduces speed error by increasing the sampling rate when the system is phase-locked. From the

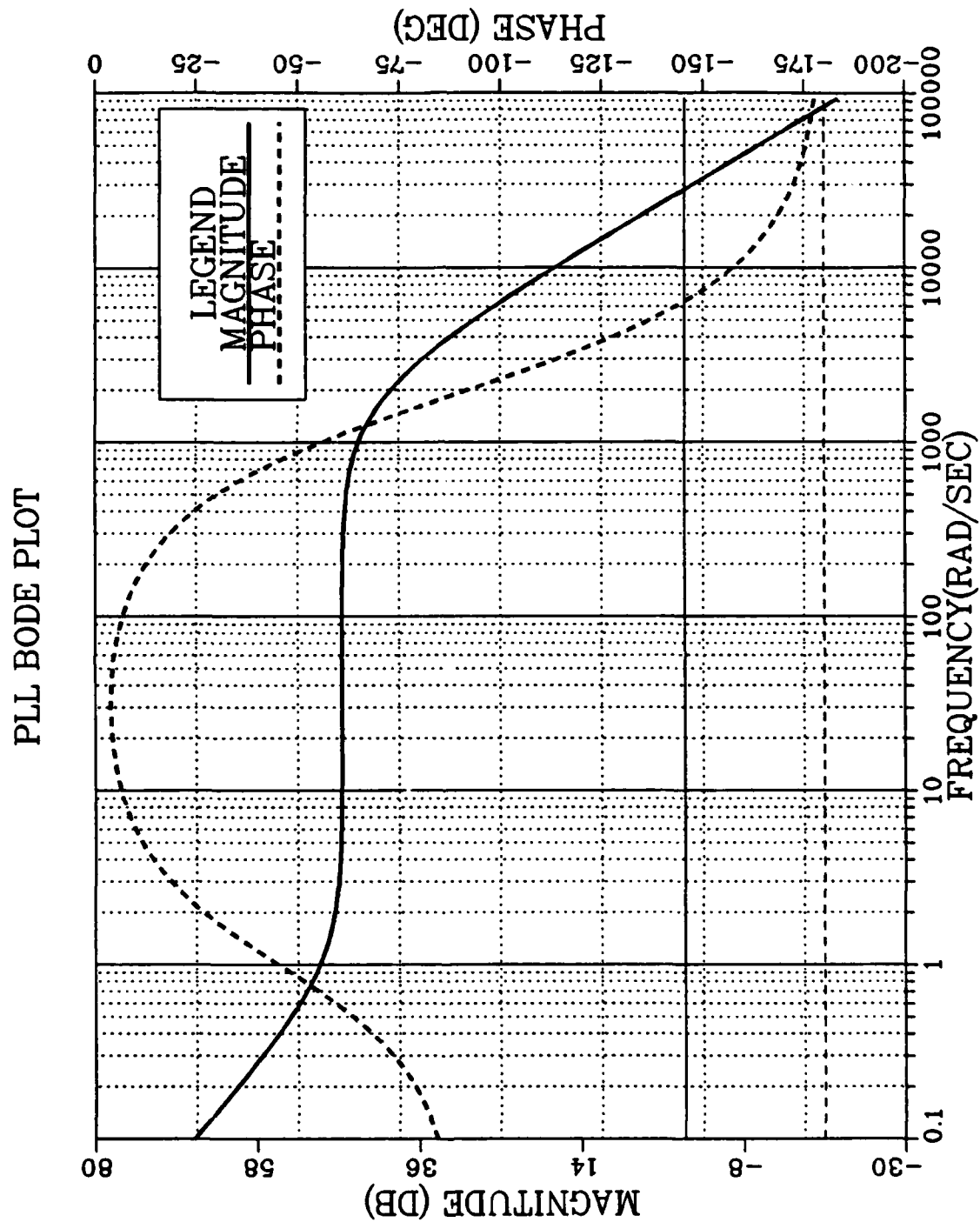


Fig. 5.16  $K_c = 0.66$ ,  $K_p = 0.66$ ,  $N = 36$ ,  $Z_f = 254$ ,  $P_f = 2540$

# PLL DAC PULSE TRAIN S1 AND S2 UNIT PULSE

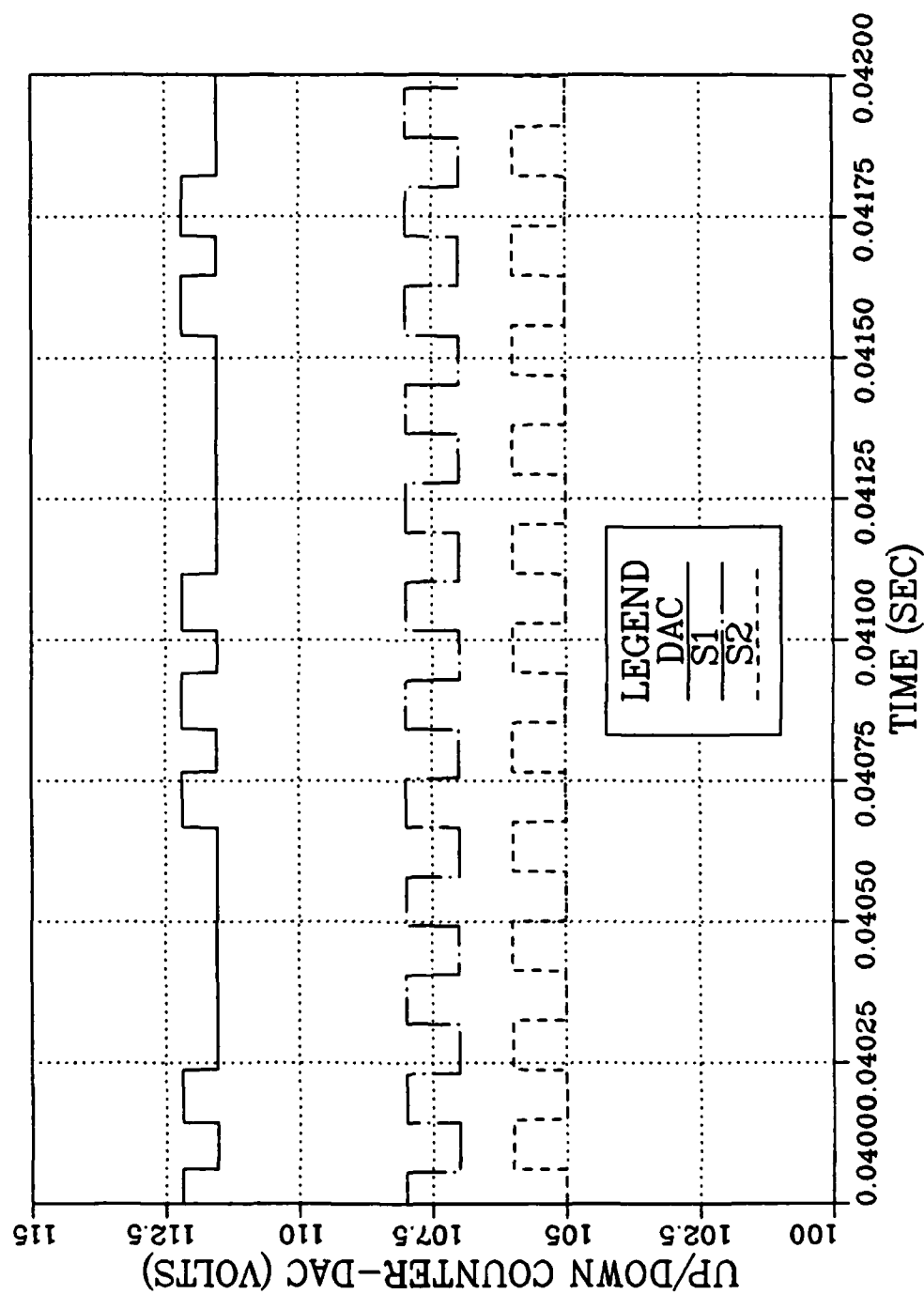


Fig. 5.17  $K_c = 0.66$ ,  $K_p = 0.66$ ,  $N = 36$ ,  $Z_f = 254$ ,  $P_f = 2540$



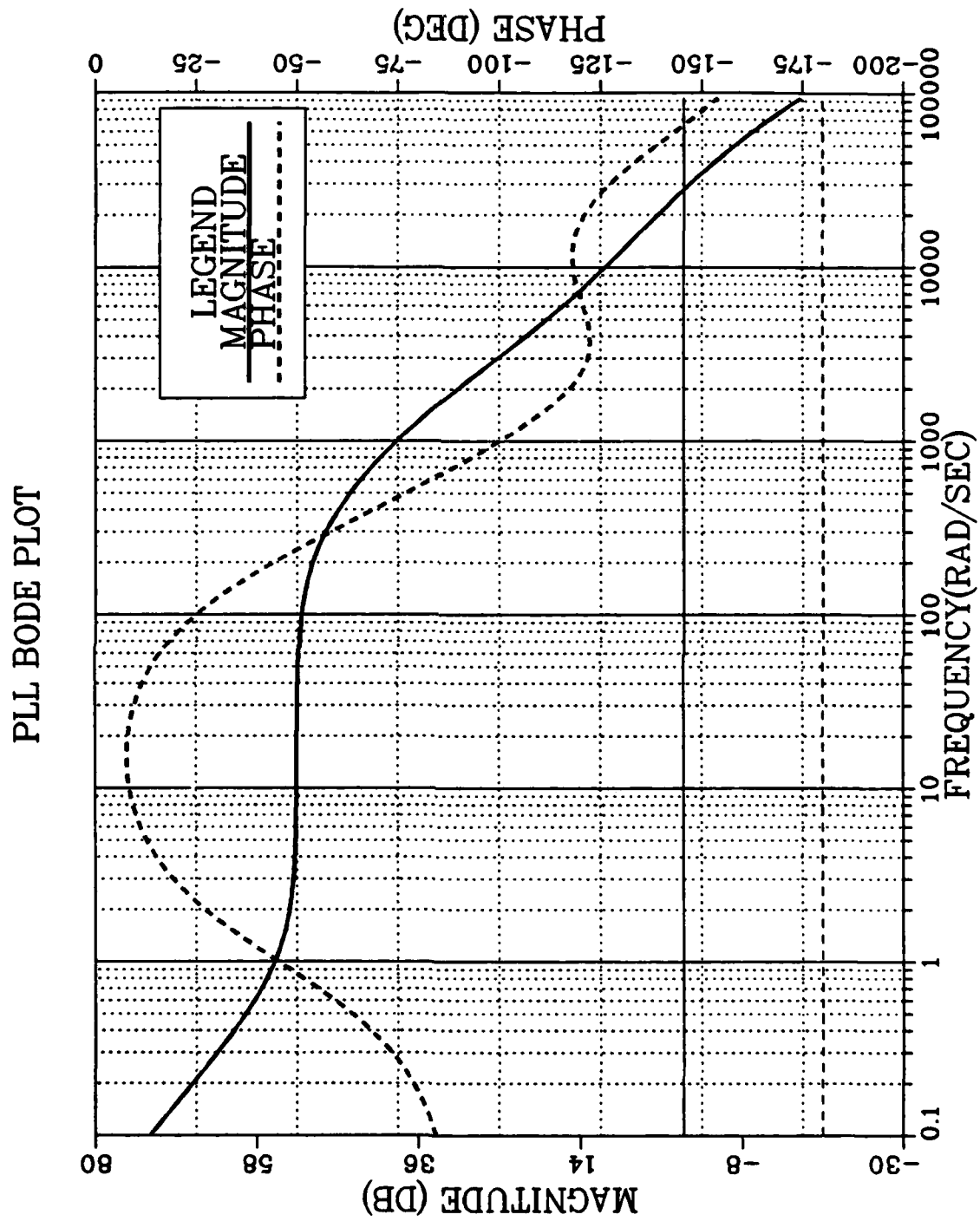


Fig. 5.18  $K_c = 0.66$ ,  $K_p = 0.66$ ,  $N = 72$ ,  $Z_f = 5000$ ,  $P_f = 50,000$

# PLL DAC PULSE TRAIN S1 AND S2 UNIT PULSE

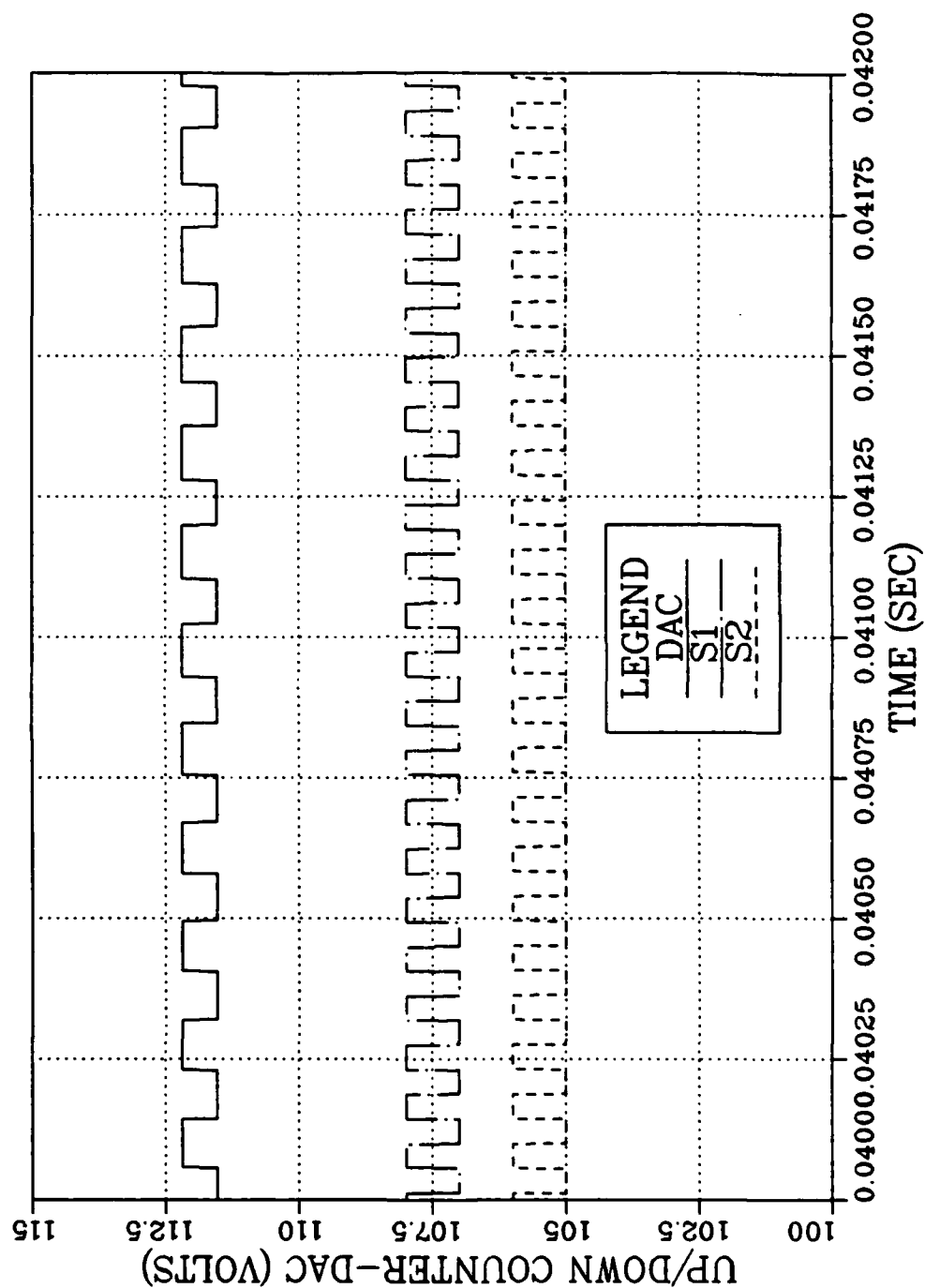


Fig. 5.19  $K_c = 0.66$ ,  $K_p = 0.66$ ,  $N = 72$ ,  $Z_f = 5000$ ,  $Pf = 50,000$

transfer equation, equation 5.13, the system bandwidth can also be increased by increasing  $K_c$ .

An increase in the counter step size ( $K_c$ ) reduces the voltage resolution (see section C.1); however, this can be compensated for by increasing the sampling rate. Increasing  $K_c$  will also increase the rate at which the counter will change.

Figure 5.20 is a Bode plot of the system with  $K_c = 1.32$ ,  $K_p = 1.32$  and  $N = 120$ . Figure 5.21 shows the up/down counter in steady state has acquired phase-lock with a motor speed of 1000 rad/sec.

An example of the controller's performance to a step input, followed by a ramp up, a ramp down, then a step down followed by a torque load, is shown in Figure 5.22. The following system parameters were used:

$$K_c = 1.32 \text{ volts/count}$$

$$K_p = 1.32 \text{ volts/(rad/sec)}$$

$$V_{\text{sat}} = \pm 50 \text{ volts}$$

$$N = 120$$

$$F(S) = 10 \cdot ((S+5000)/(S+50000))$$

The control scheme is capable of tracking the reference input over a wide range with less than 0.02% error and regulates for a torque load of 90 oz-in.

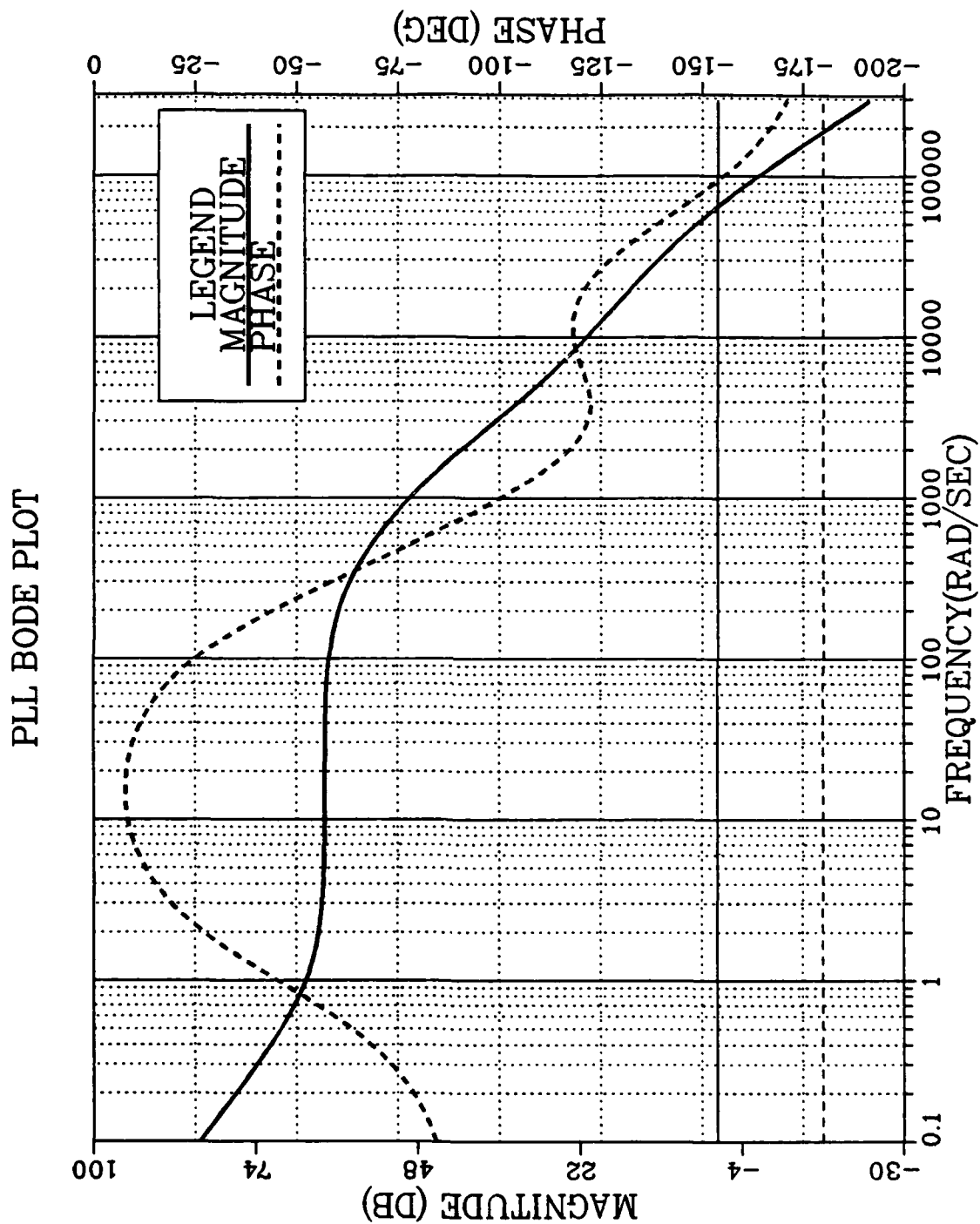


Fig. 5.20  $K_c = 1.32$ ,  $K_p = 1.32$ ,  $N = 120$ ,  $Z_f = 5000$ ,  $P_f = 50,000$

# PLL DAC PULSE TRAIN S1 AND S2 UNIT PULSE

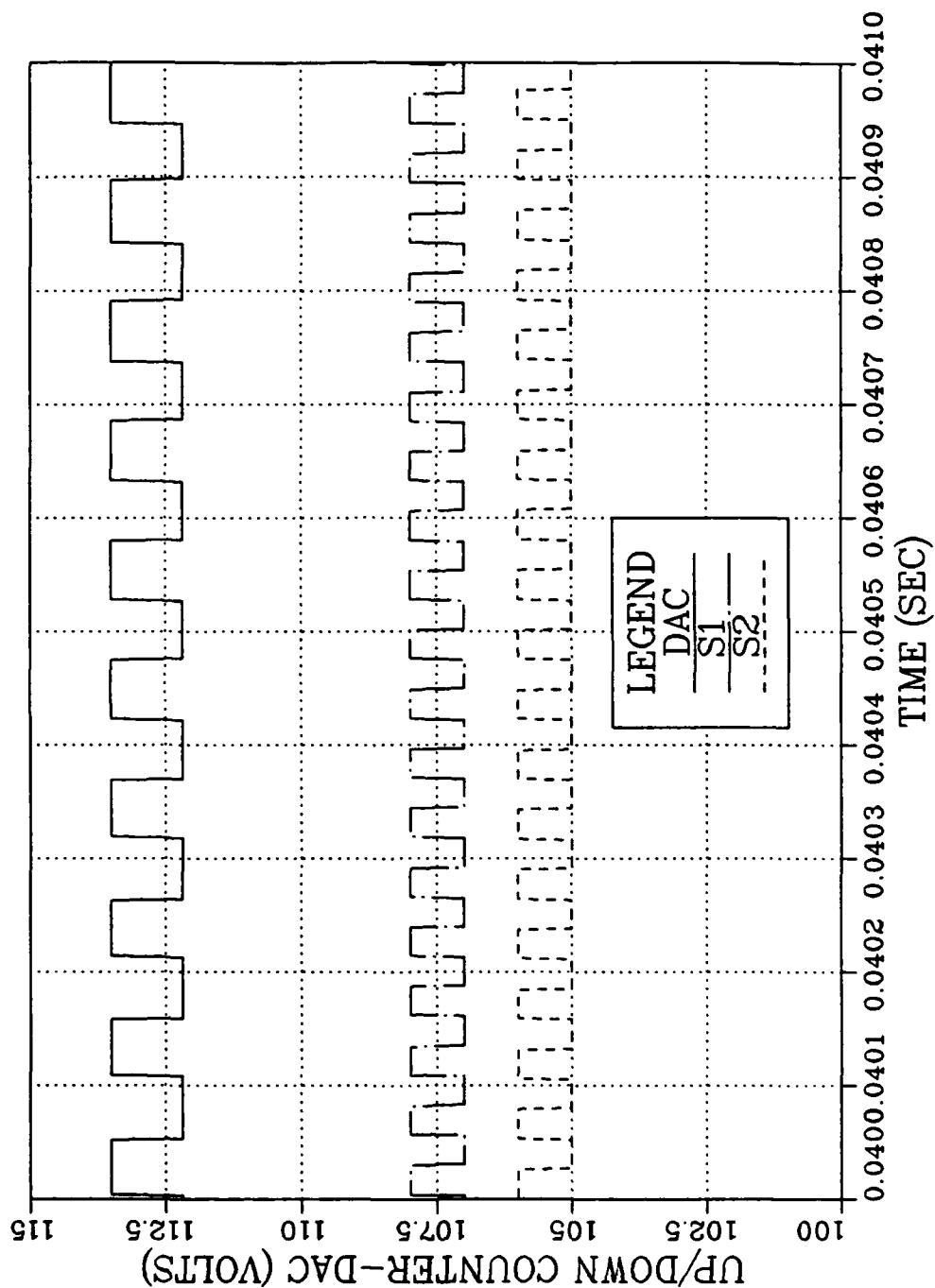


Fig. 5.21  $K_c = 1.32$ ,  $K_p = 1.32$ ,  $N = 120$ ,  $Z_f = 5000$ ,  $P_f = 50,000$

# PLL MOTOR SPEED CONTROL SPEED AND DAC VOLTS

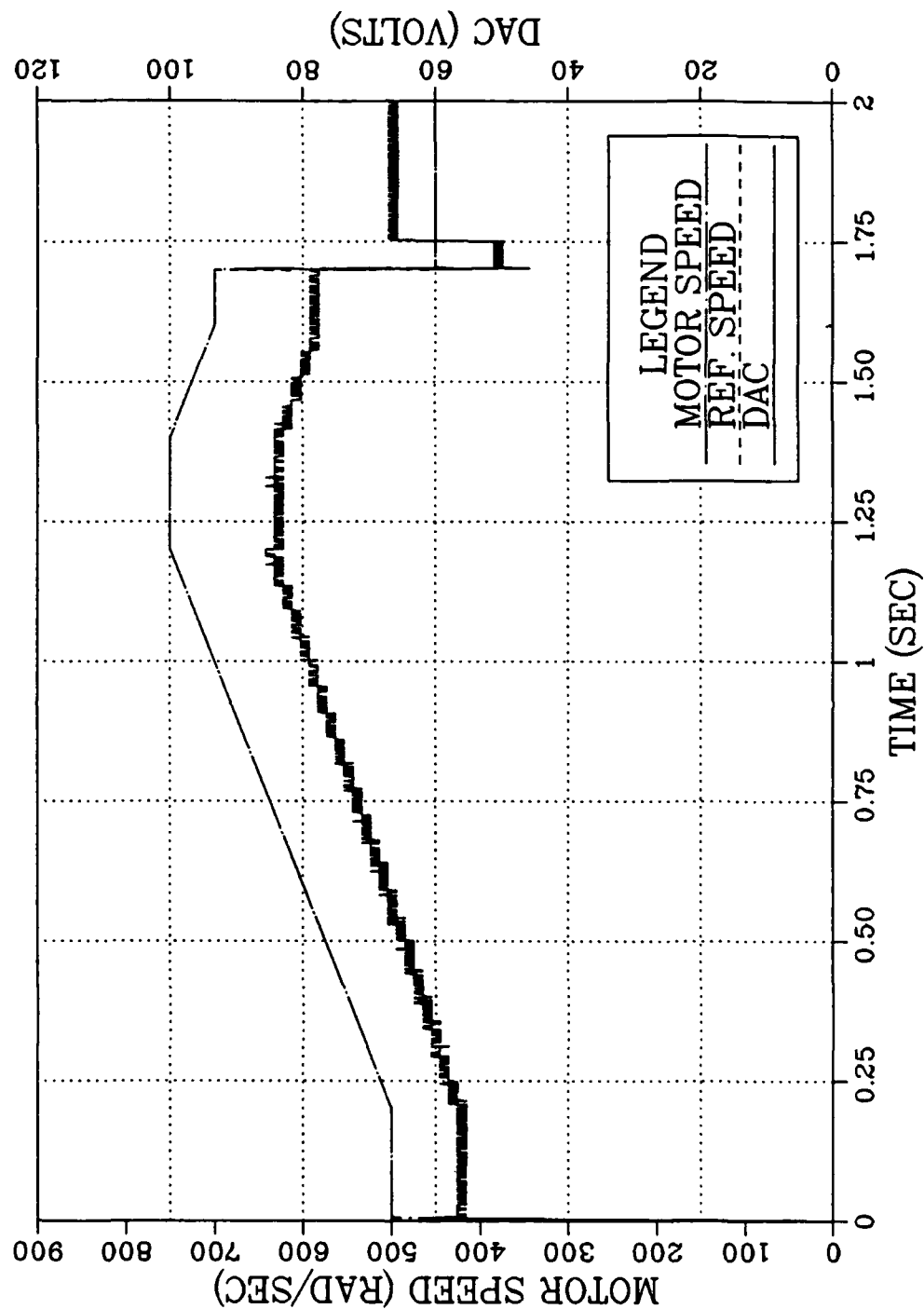


Fig. 5.22 PLL Response to Ramp and Step Inputs  
(90 oz-in torque at  $t = 1.75$ )

## VI. SUMMARY

### A. REMARKS AND CONCLUSIONS

Digital phase-locked loop has been shown to be a viable method of accurately and reliably controlling the speed of a brushless d.c. motor. The addition of logic controlled, count enable/disable, to a synchronous up/down counter was shown to improve the performance of previously proposed PLL control schemes. An exhaustive search of operating conditions demonstrated the enhanced stability of the system and its robust nature to parameter variations.

Digital computer simulation of the phase-locked loop scheme proved to be an invaluable aid in its development. However, there still exists a need to develop an accurate mathematical model.

### B. RECOMMENDATIONS FOR FURTHER STUDIES

The computer simulation model assumed an ideal digital frequency-to-voltage conversion. It is recommended that for further studies a more advanced model of the AN-210 PLL frequency-to-voltage converter be included.

The model and analysis in this thesis were developed from linear control theory. Future studies could be conducted using discrete control theory and the z-transform.

It is certainly recommended that the control scheme be implemented in hardware and tested with a specific application in mind.

## APPENDIX A

### LISTING OF MODEL PROGRAM

The program listing in this section is a basic program that simulates the action of a digital up/down counter and brushless d.c. motor. The motor that was modelled was a commercially available brushless d.c. motor.



## LISTING OF MODEL PROGRAM

70



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